SPECIALTY MEMORY PRODUCTS

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RAMTRON

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Corporate Profile and Quality Statement

Ramtron International Corporation develops, manufactures, and markets leading edge specialty memory products for a diverse range of applications. This book provides comprehensive technical information on Ramtron's FRAM® (ferroelectric RAM) and EDRAM (enhanced DRAM) product lines.

Ramtron's 69,000-square-foot headquarters, research, and manufacturing facility is located in Colorado Springs, Colorado. The facility is equipped with a Class 10 cleanroom for the production of sub-micron feature size memory products on 6-inch silicon wafers. The facility currently has a capacity of 2,600 wafers per month and can be outfitted to reach approximately 6,500 wafers per month.

Ramtron International Corporation is a U.S. public company incorporated in the state of Delaware and trades on the U.S. NASDAQ system under the symbol "RMTR".

FRAM Products

FRAM memories solve the inherent problem of volatility in microelectronic circuits by merging ferroelectric materials with conventional integrated circuitry. Ramtron's FRAM product family includes nonvolatile 4K, 16K, and 64K memories. You can use these memories as enhanced replacements in many EEPROM, NVRAM, and battery-backed SRAM applications. With the advantages of less space, lower current, fast write time, and high write endurance, we feel that you will find memory requirements in your designs that will benefit from the use of FRAM products.

EDRAM Products

In addition to ferroelectric RAM products, Ramtron also offers a family of specialty high performance 4-megabit enhanced DRAM products. The EDRAM combines a fast 35ns DRAM with an on-chip 15ns cache in a JEDEC compatible package. The EDRAM's benefits include higher system performance with lower overall system cost, power consumption, and reduced board area. The EDRAM is ideal for a variety of applications including embedded control, graphics processing cards, portable PCs, and high performance computing platforms.

Please call 1-800-545-FRAM or 1-800-545-DRAM for additional information, design assistance, or the representative nearest you.

World-class Quality Control

Ramtron takes a unique cultural approach to the issue of quality. At Ramtron, quality is not a program; it's a way of thinking and behaving. We call this approach the CLEAR Advantage Culture. It puts our customers first and emphasizes a total commitment to quality at every level of the company.

To ensure that the quality commitment is felt throughout the organization, a separate quality reporting structure exists alongside the traditional organizational structure. The focal element of the CLEAR Advantage Culture is the CLEAR Advantage Steering Committee. This is a company-wide quality committee that facilitates and nurtures the pursuit of total quality at Ramtron. The committee also works with problem-solving CLEAR Action Teams, which assume responsibility for specific quality issues being addressed through the many steps involved in bringing our customers Ramtron's advanced memories.

Through this network of quality-conscious workers and management practices, Ramtron achieves consistently high levels of quality, giving ourselves and our customers a CLEAR Advantage in memory solutions.

FM1208S FRAM® Memory

4,096-Bit Nonvolatile Ferroelectric RAM
Product Specification

1

Features

- 4,096 Bit Bytewide Nonvolatile Ferroelectric RAM
  Organized as 512 x 8
- CMOS Technology with Integrated Ferroelectric Storage Cells
- Fully Synchronous Operation
  - 200ns Read Access
  - 400ns Read/Write Cycle Time
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
- On Chip Data Protection Circuit
- 10 Year Data Retention without Power
- Single 5 Volt ±10% Supply
- Low Power Consumption
  - Active Current: 10mA
  - Standby Current: 100µA
- CMOS/TTL Compatible I/O Pins
- 24 Pin DIP and SOP Packages
- 0-70°C Ambient Operating Temperature Range

Description

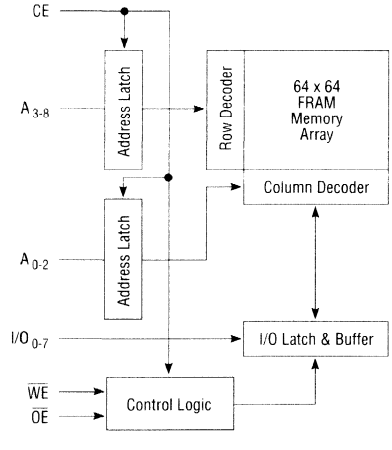
The FM1208S is a bytewide ferroelectric RAM, or FRAM® product, organized as 512 x 8. FRAM memory products from Ramtron combine the read/write characteristics of semiconductor RAM with the nonvolatile retention of magnetic storage.

This product is manufactured in a CMOS technology with the addition of integrated thin film ferroelectric storage cells developed and patented by Ramtron.

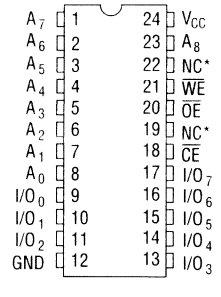
The ferroelectric cells are polarized on each read or write cycle, therefore no special store or recall sequence is required. The memory is always static and nonvolatile.

Ramtron's FRAM products operate from a single +5 volt power supply and are TTL/CMOS compatible on all inputs and outputs. The FM1208S utilizes the JEDEC standard bytewide SRAM pinout, but differ slightly in operation due to the integrated address latch.

Functional Diagram



Pin Configuration



* Must be Unconnected or Tied to GND

Device Operation

Read Operation

When $\overline{CE}$ is low and $\overline{WE}$ is high, a read operation is performed by the FRAM memory. On the falling edge of $\overline{CE}$, all address bits (A_0 - A_8) are latched into the part and the cycle is started. Data will appear on the output pins a maximum access time (t_{CA}) after the beginning of the cycle.

The designer should ensure that there are no address transitions from t_{AS} (setup time) before the falling edge of $\overline{CE}$ to t_{AH} (hold time) after it. After t_{AH}, the address pins are ignored for the remainder of the cycle. It is equally important that $\overline{CE}$ be generated such that unwanted glitches or pulses, of any duration, be prevented.

After the read has completed, $\overline{CE}$ should be brought high for the precharge interval (t_{PC}). During this period data is restored in the internal memory cells and the chip is prepared for the next read or write. FRAM memories will not operate in systems in which $\overline{CE}$ does not toggle with every access.

The $\overline{OE}$ pin may be used to avoid bus conflicts on the system bus. Only when both $\overline{CE}$ and $\overline{OE}$ are low will the FRAM memory drive its outputs. Under all other circumstances, the output drivers are held in a high impedance (High-Z) condition. Note that the internal read operation is performed regardless of the state of the $\overline{OE}$ pin.

Write Operation

When $\overline{CE}$ falls while $\overline{WE}$ is low, or $\overline{WE}$ falls while $\overline{CE}$ is low, a write operation will be performed by the FRAM memory. On the falling edge of $\overline{CE}$, as in the read cycle, the address will be latched into the part with the same setup and hold requirements. As in the read cycle, $\overline{CE}$ must be held high for a precharge interval (t_{PC}) between each access.

Data is latched into the part on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Write operations take place regardless of the state of $\overline{OE}$, however, it may need to be driven high by the system at the beginning of the cycle in order to avoid bus conflicts.

There is no long internal write delay after a write operation. Data is immediately nonvolatile and power may be removed from the part upon completion of the precharge interval following the write.

Low Voltage Protection

When V_{CC} is below 3.5V (typical), all read and write operations to the part will be ignored. For systems in which unwanted signal transitions would otherwise occur on the $\overline{CE}$ pin at or above this voltage, $\overline{CE}$ should be held high with a power supply monitor circuit.

Whenever V_{CC} rises above 3.5V, either after power up or a brownout, no read or write operation will take place until $\overline{CE}$ has been high (above V_{IH}) for at least a precharge interval (t_{PC}). When it is brought low, an access will start.

Theory of Operation

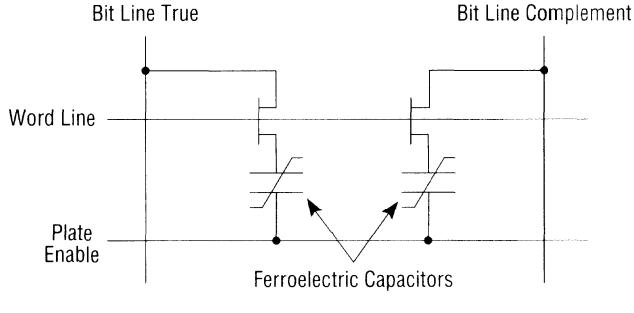
The FM1208S FRAM memory uses a patented ferroelectric technology to achieve nonvolatility. Ferroelectric material may be polarized in one direction or another with the application of an electric field, and will remain polarized when the field is removed. They are insensitive to magnetic fields.

The FM1208S is designed with a differential cell architecture, as shown in the figure below. During a read operation, the word line and plate enable lines are brought high, transferring charge from the ferroelectric storage elements to the bit lines. Nonvolatile elements polarized in the opposite direction to the field will source more charge than those polarized in the direction of the field. Sense amplifiers built into the chip compare the two charge magnitudes, producing a binary value. After the read operation, the data is then automatically re-written back into the nonvolatile elements.

During the write operation, the sense amplifiers drive the bit lines to the state of the data input pins. The word line is enabled and the place enable line is pulsed, polarizing each of the complementary nonvolatile storage elements in the appropriate direction.

The part may be read or written a total of 10 billion (10^{10}) cycles without degrading the data retention of the device. Operation of the part beyond this limit will eventually result in nonvolatile data retention failure.

FRAM Memory Cell



Absolute Maximum Ratings(1)

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	0 to +70°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Parameter	Description	Max	Test Condition
$C_{I/O}$ (2)	Input/Output Capacitance	8pF	$V_{I/O}$ = 0V
C_{IN} (2)	Input Capacitance	6pF	$V_{I/O}$ = 0V

(2) This parameter is periodically sampled and not 100% tested.

DC Operating Conditions

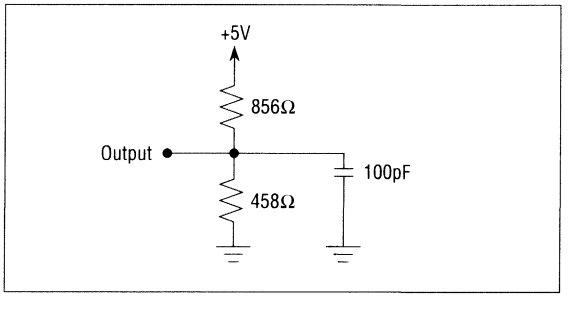
T_A = 0° to 70°C; Typical Values at 25°C

Symbol	Parameters	Min	Typ	Max	Test Condition
V_{CC}	Power Supply Voltage	4.5V	5.0	5.5V	
I_{CC1}	Power Supply Current - Active		5.0mA	10mA	V_{CC} = Max, $\overline{CE}$ Cycling at Minimum Cycle Time CMOS Input Levels and I/Os Unloaded
I_{SB1}	Power Supply Current - Standby (TTL)		200µA	1.2mA	V_{CC} = Max, $\overline{CE}$ = V_{IH}, TTL Input Levels, $I_{I/O}$ = 0mA
I_{SB2}	Power Supply Current - Standby (CMOS)		10µA	100µA	V_{CC} = Max, $\overline{CE}$ = V_{CC}, CMOS Input Levels, $I_{I/O}$ = 0mA
I_{IL}	Input Leakage Current			10µA	V_{IN} = GND to V_{CC}
I_{OL}	Output Leakage Current			10µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	-1V		0.8V	
V_{IH}	Input High Voltage	2.0V		V_{CC} + 1V	
V_{OL}	Output Low Voltage			0.4V	I_{OL} = 4.2mA
V_{OH}	Output High Voltage	2.4V			I_{OH} = -2mA

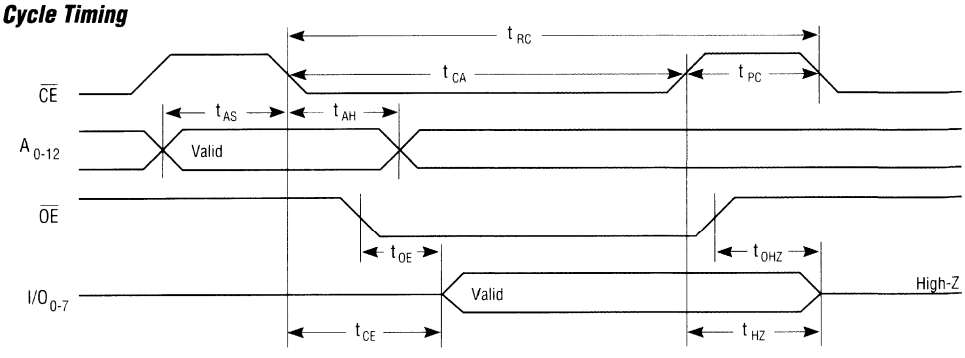
AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	0 to 3 V
Input Rise and Fall Time	10ns
Input and Output Timing Levels	1.5V

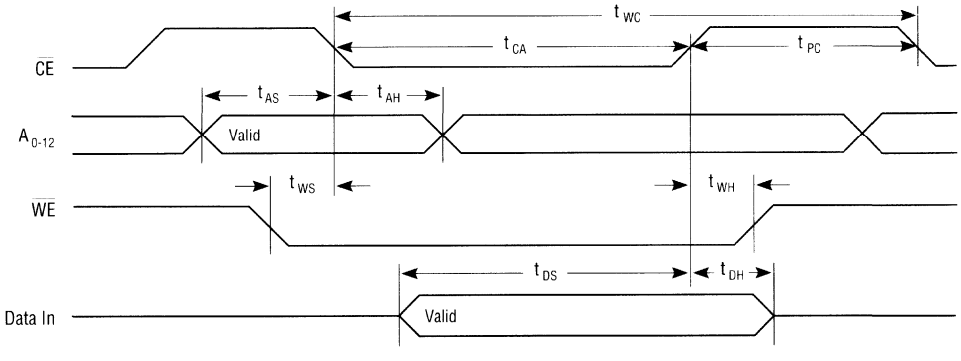
Equivalent AC Test Load Circuit



Read Cycle Timing

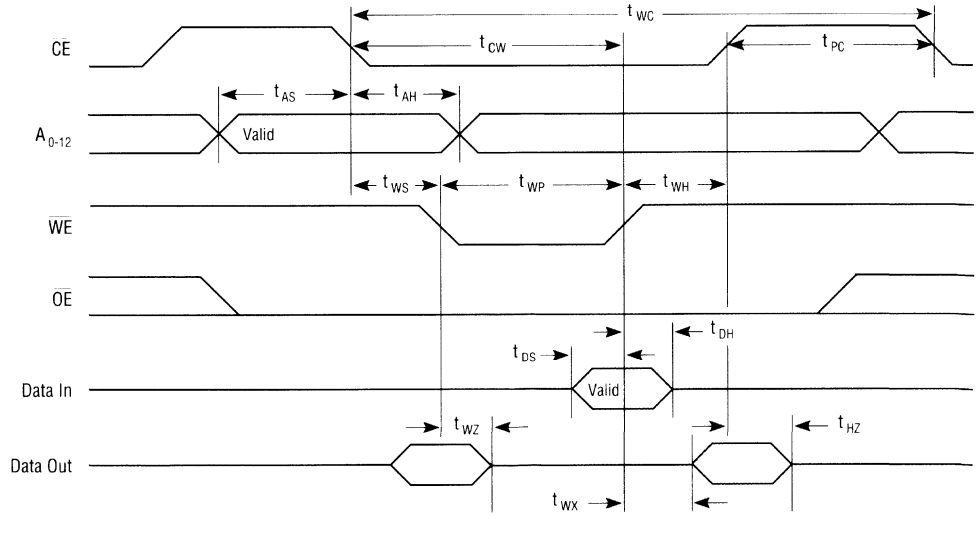


$\overline{CE}$ Controlled Write(5)



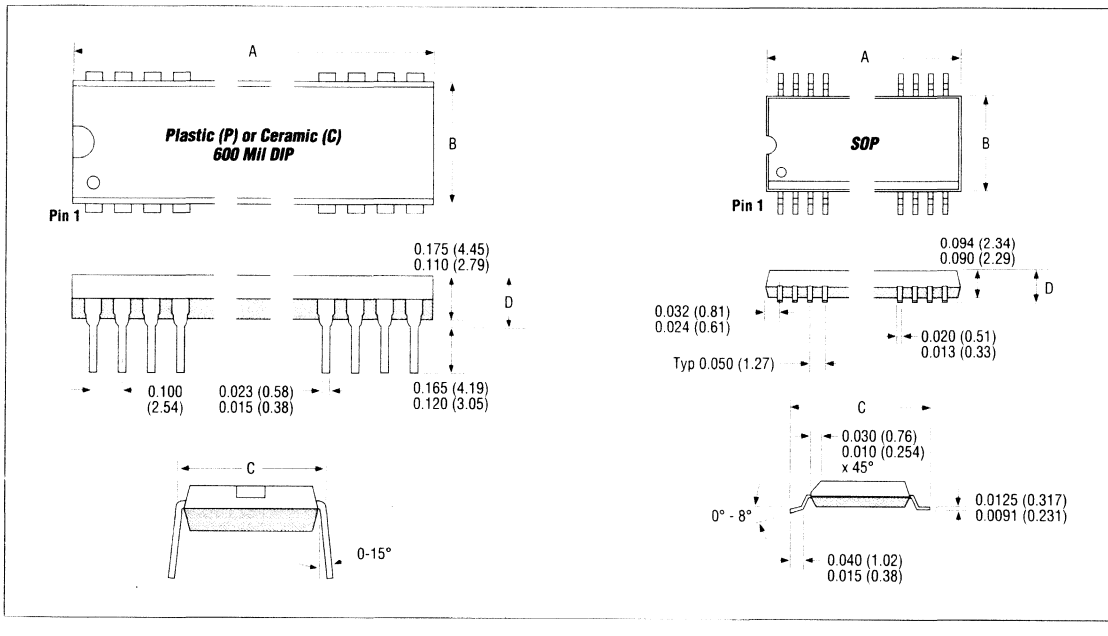
(5) State of $\overline{OE}$ does not affect operation of device for this cycle.

$\overline{WE}$ Controlled Write

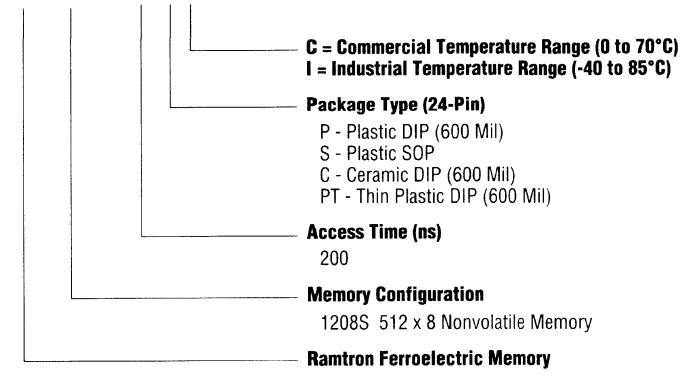


Packaging Information

Package	Type	Dimensions in Inches (Millimeters)			
		FM1208S 24-Pin			
		A	B	C	D
Plastic/Ceramic 600 Mil DIP	P/PT/C	1.240 (32.64) 1.285 (31.50)	0.598 (15.19) 0.514 (13.06)	0.620 (15.75) 0.590 (14.99)	0.225 (5.72) 0.140 (3.56)
Plastic SOP	S	0.614 (15.59) 0.598 (15.19)	0.300 (7.62) 0.287 (7.29)	0.416 (10.57) 0.398 (10.11)	0.105 (2.65) 0.093 (2.35)



Ordering Information



FM24C04 FRAM® Serial Memory

Product Specification

1

Features

- 4,096-Bit Nonvolatile Ferroelectric RAM Organized as 512w x 8b
- Very Low Power CMOS Technology
  - 100µA Active (Read or Write)
  - 25µA Standby Over Commercial Temperature Range
- Reliable Thin Film Ferroelectric Technology
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
  - 10 Year Data Retention
- High Performance
  - No Write Delay
  - 512 Byte Sequential Write
  - 47ms Full Chip Write
- Two Wire I²C Serial Interface
  - Direct Replacement for Xicor X24C04
- Hardware Write Protection
- True 5V Only Operation
- 8 Pin Mini-DIP and SOIC Packages
- -40° to +85°C Operating Range

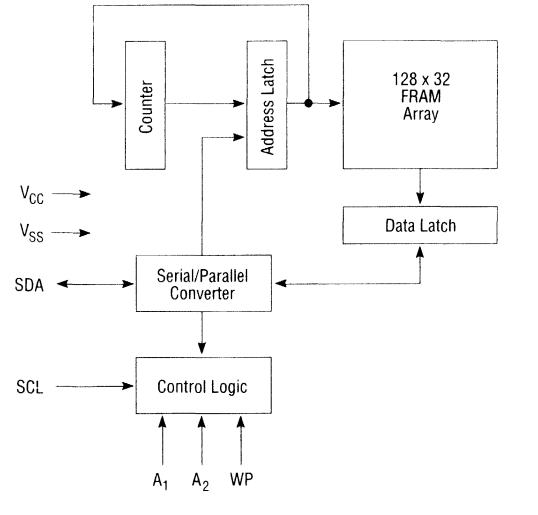
Description

The Ramtron FM24C04 ferroelectric random access memory, or FRAM® memory provides nonvolatile data integrity in a compact package. A two wire serial interface provides access to any byte within the memory while reducing the cost of the processor interface. The FM24C04 is useful in a wide variety of applications for the storage of configuration information, user programmable data/features, and calibration data.

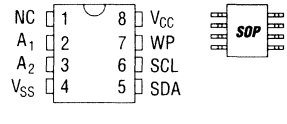
With Ramtron s ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra page mode control, or high voltage pins. The technology is designed for highly reliable operation, offering extended endurance and 10 year data retention.

The part uses the industry standard two wire protocol for serial chip communication and is pin compatible with a number of parts from other vendors. Up to 16Kbits of FRAM memory may be connected on a single bus, comprised of multiple 24C04 parts. It is available in 300 mil mini-DIP and 150 mil SOP packages.

Functional Diagram



Pin Configurations



Pin Names	Function
A_1 - A_2	Device Address
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage

 1850 Ramtron Drive, Colorado Springs, CO 80921
Telephone (800) 545-FRAM, (719) 481-7000 **Fax** (719) 488-9095

Absolute Maximum Ratings

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	-40°C to +85°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
D.C. Output Current	5mA
Lead Temperature (Soldering, 10 Seconds)	300°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Operating Conditions

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	V_{CC} Supply Current		60	100	µA	SCL @ 100KHz, Read or Write SCL CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{SB}(2)	Standby Current 0°C to 70°C		8	25	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{SB}(2)	Standby Current -40°C to 85°C		16	60	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}	Input Low Voltage	-1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3mA

(1) Typical values are measured at 25°C, 5.0V.
(2) Must perform a stop command prior to measurement.

Endurance and Data Retention

Parameter	Min	Max	Units
Endurance	10 Billion		R/W Cycles
Data Retention	10		Years

Power-Up Timing (3)

Symbol	Parameter	Max	Units
t_{PUR}(3)	Power Up to Read Operation	1	µs
t_{PUW}(3)	Power Up to Write Operation	1	µs

(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (A_{1-2}, SCL, WP)	6	pF	V_{IN} = 0V

(4) This paramter is periodically sampled and not 100% tested.

Pin Descriptions

SCL — Serial Clock

When high, the SCL clocks data into and out of the FM24C04. It is an input only.

SDA — Serial Data Address

This bi-directional pin is used to transfer addresses to the FM24C04 and data to or from the FM24C04. It is an open drain output and intended to be wire-ORed with all other devices on the serial bus using an external pull-up resistor.

A_1, A_2 — Address Bits 1 and 2

The A_1 and A_2 inputs set the device address for this particular FM24C04. If the state of A_1 and A_2 matches that within the slave address, then this FM24C04 will respond to the command. These pins must be connected to either V_{CC} or V_{SS}.

WP — Write Protect

If tied to V_{CC}, write operations into the upper half of the memory (bank select A_0 set to 1 in the slave address) will be disabled. Read and write operations to the lower portion of memory will proceed normally. If the write protection feature is not desired, this pin must be tied to V_{SS}.

Bus Protocol

The FM24C04 employs a bi-directional two wire bus protocol designed to support multiple bus slaves with a minimum of processor I/O pins. Figure 1 shows a typical system configuration connecting a microcontroller with two FM24C04 devices. Up to four FM24C04 devices can be connected on a single bus.

By convention, any device sending data onto the bus is the transmitter, while the device that is getting the data is the receiver. The device controlling the bus is the master and provides the clock signal for all operations. Devices being controlled are the slaves. The FM24C04 is always a slave device.

Transitions or states on the SDA and SCL lines denote one of four conditions: a *start*, *stop*, *data bit*, or *acknowledge*. Figure 2 shows the signaling for these conditions, while the following four sections describe their function.

Figure 3 shows the detailed timing specifications for the bus. Note that all SCL specifications and the *start* and *stop* specifications apply to both read and write operations. They are shown on one or the other for clarity. Also, the write timing specifications apply to all transmissions to the FM24C04, including the slave and word address, as well as write data sent to the FM24C04 from the bus master.

Figure 1. Typical System Configuration

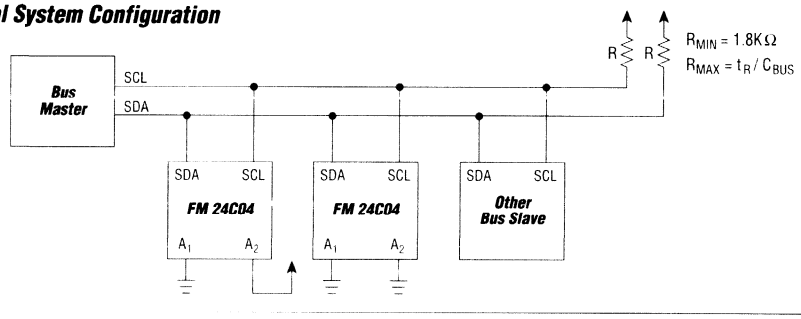


Figure 2. Data Transfer Protocol

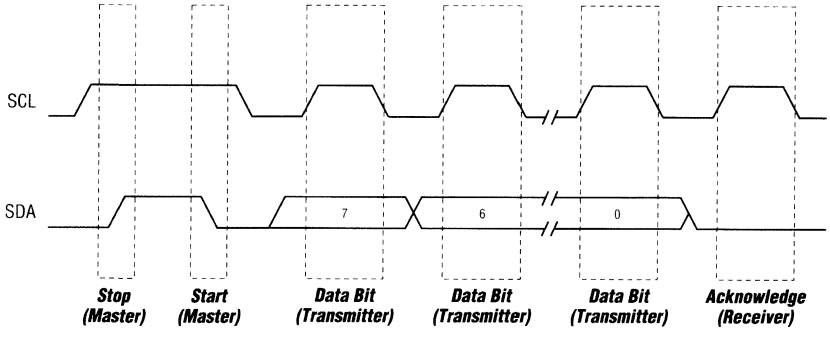
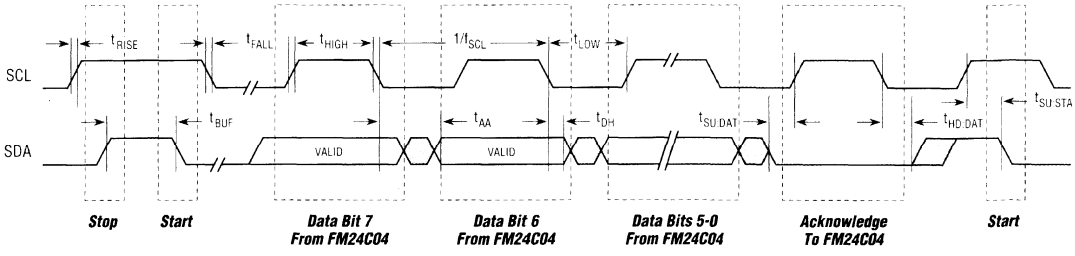
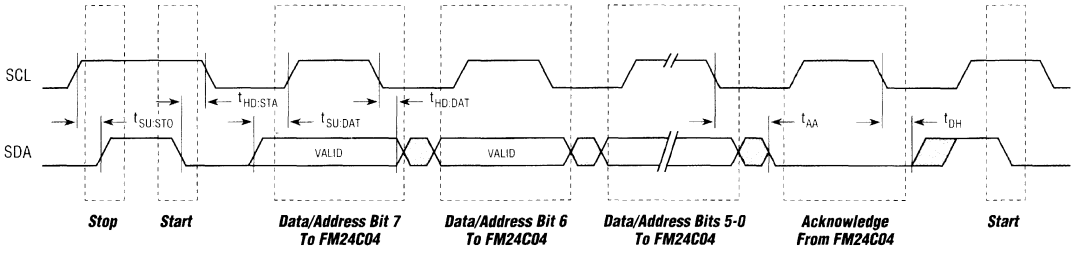


Figure 3. Bus Timing

Read



Write



Notes:
(1) All start and stop timings apply to both read and write cycles identically.
(2) Clock specifications same for both read and write.
(3) Write timing specifications apply to slave address, word address, and write data.

Read and Write Cycle AC Parameters

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		50	ns
t_{AA}	SCL Low to SDA Data Out Valid		3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_{RISE}	SDA and SCL Rise Time		1	µs
t_{FALL}	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.0		µs
t_{DH}	Data Out Hold Time (From SCL @ V_{IL})	0		ns

Start Condition

A *start* condition is indicated to the FM24C04 when there is a high to low transition of SDA while SCL is high. All commands to the FM24C04 must be preceded by a *start*. In addition, a *start* condition occurring at any point within an operation will abort that operation and ready the FM24C04 to start a new one.

Stop Condition

A *stop* condition is indicated to the FM24C04 when there is a low to high transition of SDA while SCL is high. All operations to the FM24C04 must end with a *stop*. In addition, any operation will be aborted at any point when this condition occurs.

Data/Address Transfers

Data/address transfers take place during the period when SCL is high. Except under the two conditions described above, the state of the SDA line may not change while SCL is high. Address transfers are always sent to the FM24C04, while data transfers may either be sent to the FM24C04 (for a write) or to the bus master (for a read).

Acknowledge

Acknowledge transfers take place on the ninth clock cycle after each eight-bit address or data transfer. During this clock cycle, the transmitter will release the SDA bus to allow the receiver to drive the bus low to acknowledge receipt of the byte.

Device Operation

Low Voltage Protection

When powering up, the FM24C04 will automatically perform an internal reset and await a *start* signal from the bus master. The bus master should wait T_{PUR} (or T_{PUW}) after V_{CC} reaches 4.5V before issuing the *start* for the first read or write access. Additionally, whenever V_{CC} falls below 3.5V (typical), the part goes into its low voltage protection mode. In this mode, all accesses to the part are inhibited and the part performs an internal reset. If an access was in progress when the power supply fails, it will be automatically aborted by the FM24C04. When power rises back above 4.5V, a *start* signal must be issued by the bus master to initiate an access.

Slave Address

Following a *start*, the FM24C04 will expect a slave address byte to appear on the bus. This byte consists of four parts as shown in Figure 4.

- Bits 7 through 4 are the device type identifier which must be binary 1010 as shown.
- Bits 2 and 3 are the device address. If bit 2 matches the state of the A_1 pin and bit 3 matches the state of the A_2 pin, then the part will be selected.
- Bit 1 is the page select. If set to 1, then the upper 256 bytes of memory (addresses hex 100 through 1ff) will be accessed, while the lower block will be accessed if it is 0.
- Bit 0 is the read/write bit. If set to a 1, a read operation is being performed by the master; otherwise, a write is intended.

Word Address

After a slave device *acknowledges* the slave address on a write operation, the master will place the word address on the bus. This byte, in addition to the page select bit from the slave address, forms the address of the byte within the memory that is to be written. This nine-bit value is latched in the internal address latch. There is no word address specified during a read operation.

During the transmission of each data byte and before the acknowledge cycle, the address in the internal latch is incremented to allow the following byte to be accessed immediately. When the last byte in the memory is accessed (at address hex 1ff), the address is reset to 0. There is no alignment requirement for the first byte of a block cycle — any address may be specified. There is also no limit to the number of bytes that may be accessed in a single read or write operation.

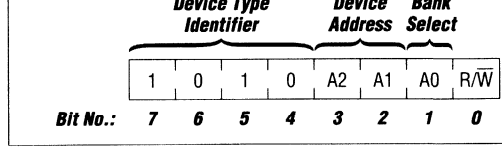
Data Transfer

After all address bytes have been transmitted, data will be transferred between the FM24C04 and the bus master. In the case of a read, the FM24C04 will place each of the eight bits on the bus and then wait for an acknowledge from the bus master before performing a read on the subsequent address. For a write operation, the FM24C04 will accept eight bits from the bus master and then drive the acknowledge on the bus.

All data and address bytes are transmitted most significant bit (bit 7) first.

After the acknowledge of a data byte transfer, the bus master may either begin another read or write on the subsequent byte, issue a *stop* command to terminate the block operation, or issue a *start* command to terminate the current operation and start a new one.

Figure 4. Slave Address



Write Operations

All write operations start with a slave and word address transmission to the FM24C04. In the slave address, bit 0 should be set to a 0 to denote a write operation. After they are acknowledged, the bus master transmits each data byte(s) to the FM24C04. After each byte, the FM24C04 will generate an acknowledge signal. Any number of bytes may be written in a single write sequence. After the last byte in the memory (address hex 1ff) is written, the address counter wraps around to zero so that the subsequent byte written will be the first (address 0).

There is no write delay on the FM24C04. Any operation, either a read or write to some other address, may immediately follow a write. Acknowledge polling, a sequence used with EEPROM devices to let the bus master know when a write cycle is complete, will return done immediately (the FM24C04 will acknowledge the first correct slave address).

If a write cycle must be aborted (with a *start* or *stop* condition), this should take place *before* the transmission of the eighth bit in order that the memory not be altered.

The write protect (WP) pin on the FM24C04 allows the upper half of the memory array (addresses hex 100 through 1ff) to be protected against accidental modification. When the pin is tied to V_{CC}, slave and word addresses targeted at the FM24C04 will still be acknowledged, but no acknowledge will occur on the data cycle if the address is in the upper half. In addition, no address incrementing occurs when writes are attempted to this half of the memory. If the write protection feature is not desired, this pin must be tied to V_{SS}.

Figure 5. Byte Write

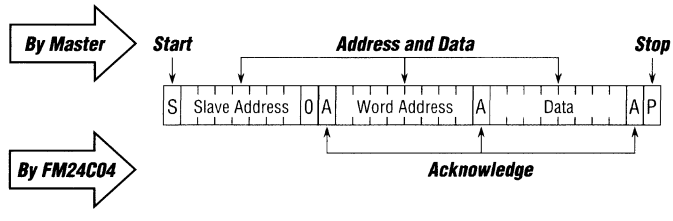
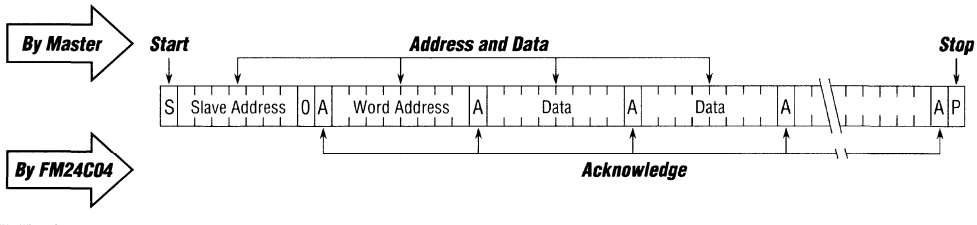


Figure 6. Multiple Byte Write



Read Operations

Current Address or Sequential Read

Sequential read operations take place from the address currently held in the internal address latch, and so require only that the bus master provide a slave address transfer before the FM24C04 begins the transfer of data to the master. In this slave address, bit 0 should be set to a 1 to denote a read operation. Note that the MSB of the nine-bit internal address latch is specified by the slave address word, and is therefore *always* set during a read, regardless of which page the previous access referenced.

One or multiple bytes may be read from the FM24C04 in a single read operation. After the final byte has been read, the bus master signifies the end of the read sequence by failing to issue an acknowledge, or issuing a *stop* or *start* command. After the last byte in the memory (address hex 1ff) is read, the address counter wraps around to zero so that the subsequent byte to be read will be the first location in the memory (address 0). These sequences are shown below in Figures 7 and 8.

Selective (Random) Read

Selective, or random, read operations are possible on the FM24C04 by using the first two bytes of the *write* operation to load the internal address. The slave address for the part is sent out with bit 0 ($R/\overline{W}$) set to 0 to denote a write operation, and the word address is set to specify the least significant 8 bits of the desired address.

After the FM24C04 acknowledges this word address, the bus master should abort the *write* and begin the read with a *start* command. A new slave address is then sent out, this time with the $R/\overline{W}$ bit set to 1. Following the slave address and acknowledge, the FM24C04 will immediately begin transmission of the requested data. Figure 9 shows this operation.

Figure 7. Current Address Read

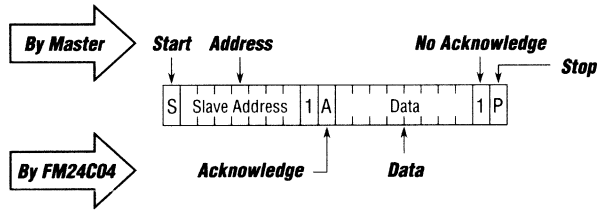


Figure 8. Sequential Read

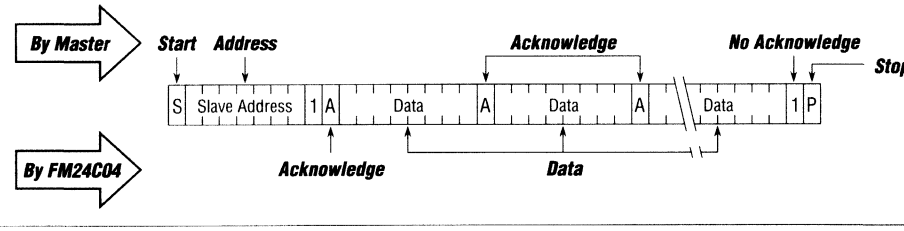
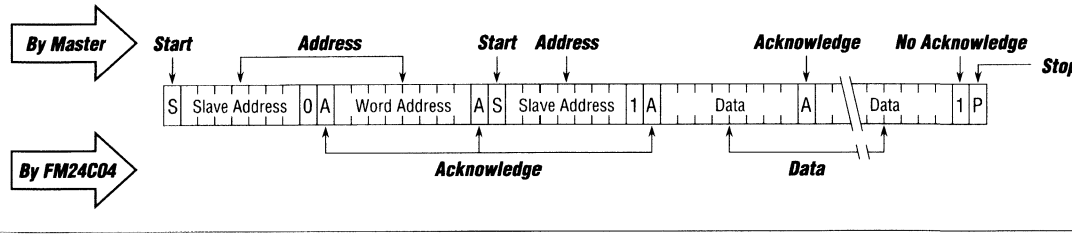
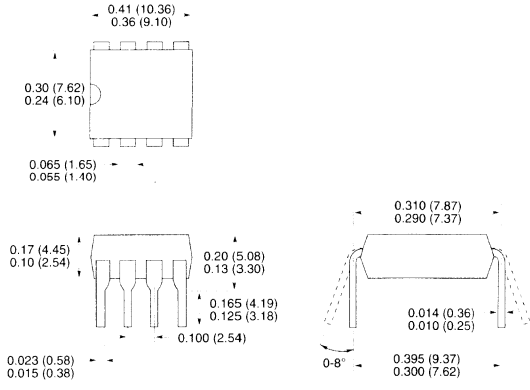


Figure 9. Selective Read

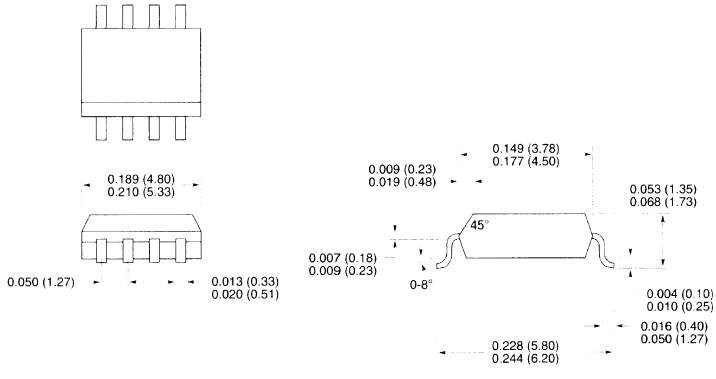


Packaging Information

8-Pin Plastic or Ceramic DIP



8-Pin SO (JEDEC)



Ordering Information

FM 24C04 - PS

Package Type (8-Pin)
PS - Plastic Skinny DIP
PT - Thin Plastic Skinny DIP
S - Plastic SOP
C - CERDIP

4K Serial FRAM Memory

Ramtron Ferroelectric Memory

FM24C16 FRAM® Serial Memory

Product Preview

1

Features

- 16Kbit Nonvolatile Ferroelectric RAM Organized as 2,048 x 8
- Very Low Power CMOS Technology
  - 100µA Active (Read or Write)
  - 25µA Standby Over Commercial Temperature Range
- Reliable Thin Film Ferroelectric Technology
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
  - 10 Year Data Retention
- High Performance
  - No Write Delay
  - 2Kbyte Sequential Write
- Two Wire I²C Serial Interface
  - 100KHz and 400KHz Modes
  - Direct Replacement for Xicor X24C16
- Hardware Write Protection
- True 5V Only Operation
- 8-Pin Mini DIP and SOIC Packages
- -40° to +85°C Operating Range

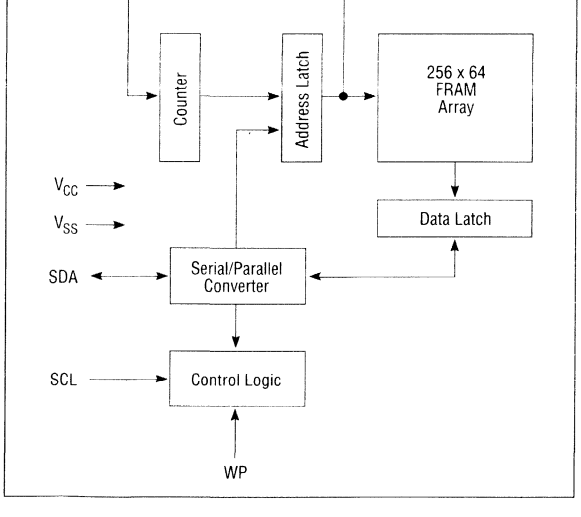
Description

Ramtron's FM24C16 ferroelectric random access memory, or FRAM® memory provides nonvolatile data integrity in a compact package. A two wire serial interface provides access to any byte within the memory while reducing the cost of the processor interface. The FM24C16 is useful in a wide variety of applications for the storage of configuration information, user programmable data/features, and calibration data.

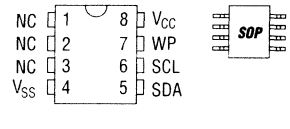
With Ramtron's ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra page mode control, or high voltage pins. The technology is designed for highly reliable operation, offering extended endurance and 10 year data retention.

The part uses the industry standard two wire protocol for serial chip communication and is pin compatible with a number of parts from other vendors. It is available in 300 mil mini-DIP and 150 mil SOP packages.

Functional Diagram



Pin Configurations



Pin Names	Function
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage

 1850 Ramtron Drive, Colorado Springs, CO 80921
***Telephone** (800) 545-FRAM, (719) 481-7000 **Fax** (719) 488-9095*
R2 February 1994

Absolute Maximum Ratings

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	-40°C to +85°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
D.C. Output Current	5mA
Lead Temperature (Soldering, 10 Seconds)	300°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Operating Conditions

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	V_{CC} Supply Current		60	100	µA	SCL @ 100KHz, Read or Write SCL CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{CC}	V_{CC} Supply Current		180	300	µA	SCL @ 400KHz, Read or Write SCL CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{SB}(2)	Standby Current 0 to 70°C		8	25	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{SB}(2)	Standby Current -40 to 85°C		16	60	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}	Input Low Voltage	-1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage			0.4	V	I_{OL} = 3mA
V_{OL2}	Output Low Voltage			0.6	V	I_{OL} = 6mA
V_{HYS}	Input Hysteresis	V_{CC} x .05			V	

(1) Typical values are measured at 25°C, 5.0V.
(2) Must perform a stop command prior to measurement.

Endurance and Data Retention

Parameter	Min	Max	Units
Endurance	10 Billion		R/W Cycles
Data Retention	10		Years

Power-Up Timing (3)

Symbol	Parameter	Max	Units
t_{PUR}(3)	Power Up to Read Operation	1	µs
t_{PUW}(3)	Power Up to Write Operation	1	µs

(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (SCL, WP)	6	pF	V_{IN} = 0V

(4) This paramter is periodically sampled and not 100% tested.

Pin Descriptions

SCL — Serial Clock

When high, the SCL clocks data into and out of the FM24C16. It is an input only. This input is built with a Schmitt trigger to provide increased noise immunity.

SDA — Serial Data Address

This bi-directional pin is used to transfer addresses to the FM24C16 and data to or from the FM24C16. It is an open drain output and intended to be wire-ORed with all other devices on the serial bus using an external pull-up resistor. The input circuitry on this pin is built with a Schmitt trigger to reduce noise sensitivity. The output section incorporates slope control for the falling edges.

WP — Write Protect

If tied to V_{CC}, write operations into the upper half of the memory (bank select A_2 set to 1 in the slave address) will be disabled. Read and write operations to the lower portion of memory will proceed normally. If the write protection feature is not desired, this pin must be tied to V_{SS}.

Bus Protocol

The FM24C16 employs a bi-directional two wire bus protocol requiring a minimum of processor I/O pins. Figure 1 shows a typical system configuration connecting a microcontroller with an FM24C16 and another I²C bus slave.

By convention, any device sending data onto the bus is the transmitter, while the device that is getting the data is the receiver. The device controlling the bus is the master and provides the clock signal for all operations. Devices being controlled are the slaves. The FM24C16 is always a slave device.

Transitions or states on the SDA and SCL lines denote one of four conditions: a *start*, *stop*, *data bit*, or *acknowledge*. Figure 2 shows the signaling for these conditions, while the following four sections describe their function.

Figure 3 shows the detailed timing specifications for the bus. Note that all SCL specifications and the *start* and *stop* specifications apply to both read and write operations. They are shown on one or the other for clarity. Also, the write timing specifications apply to all transmissions to the FM24C16, including the slave and word address, as well as write data sent to the FM24C16 from the bus master.

Start Condition

A *start* condition is indicated to the FM24C16 when there is a high to low transition of SDA while SCL is high. All commands to the FM24C16 must be preceded by a *start*. In addition, a *start* condition occurring at any point within an operation will abort that operation and ready the FM24C16 to start a new one.

Figure 1. Typical System Configuration

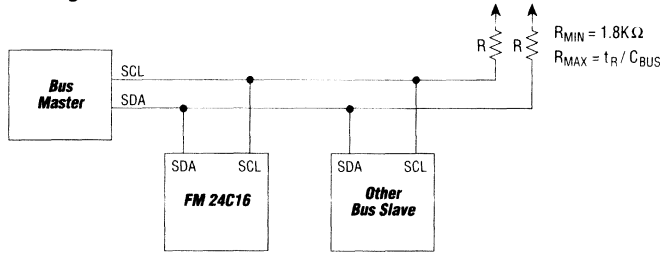


Figure 2. Data Transfer Protocol

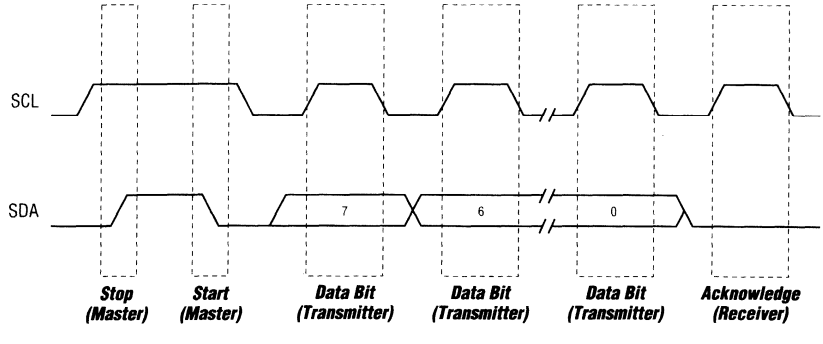
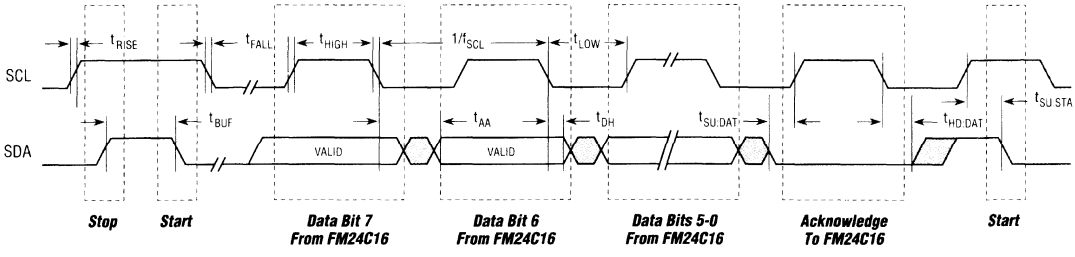
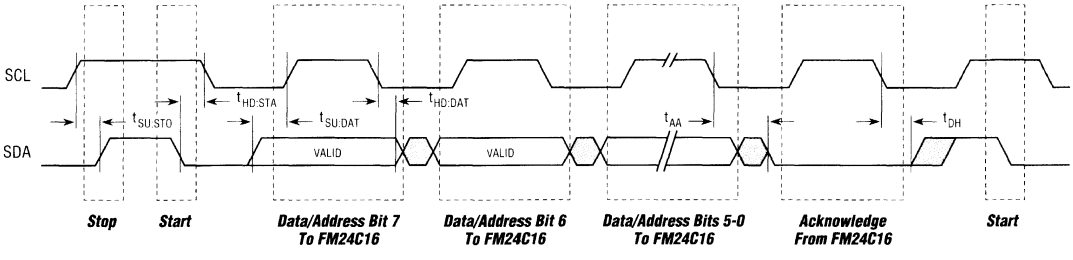


Figure 3. Bus Timing

Read



Write



Notes:
(1) All start and stop timings apply to both read and write cycles identically.
(2) Clock specifications are the same for both read and write.
(3) Write timing specifications apply to slave address, word address, and write data.

Read and Write Cycle AC Parameters

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	KHz
T_{SP}	Noise Suppression Time Constant at SCL, SDA Inputs		50		50	ns
t_{AA}	SCL Low to SDA Data Out Valid		3		0.9	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.3		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_{RISE}	SDA and SCL Rise Time		1000	$20+0.1C_b$ (4)	300	ns
t_{FALL}	SDA and SCL Fall Time		300	$20+0.1C_b$ (4)	300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.0		0.6		µs
t_{DH}	Data Out Hold Time (From SCL @ V_{IL})	0		0		ns
t_{OF}	Output Fall Time (V_{IH} Min to V_{IL} Max)		250	$20+0.1C_b$ (4)	250	ns

(4) C_b = Total Capacitance of One Bus Line in pF

Stop Condition

A *stop* condition is indicated to the FM24C16 when there is a low to high transition of SDA while SCL is high. All operations to the FM24C16 should end with a *stop*. In addition, any operation will be aborted at any point when this condition occurs.

Data/Address Transfers

Data/address transfers take place during the period when SCL is high. Except under the two conditions described above, the state of the SDA line may not change while SCL is high. Address transfers are always sent to the FM24C16, while data transfers may either be sent to the FM24C16 (for a write) or to the bus master (for a read).

Acknowledge

Acknowledge transfers take place on the ninth clock cycle after each eight-bit address or data transfer. During this clock cycle, the transmitter will release the SDA bus to allow the receiver to drive the bus low to acknowledge receipt of the byte.

If the receiver does not acknowledge any byte, the operation is aborted.

Device Operation

Low Voltage Protection

When powering up, the FM24C16 will automatically perform an internal reset and await a *start* signal from the bus master. The bus master should wait T_{PUR} (or T_{PUW}) after V_{CC} reaches 4.5V before issuing the *start* for the first read or write access. Additionally, whenever V_{CC} falls below 3.5V (typical), the part goes into its low voltage protection mode. In this mode, all accesses to the part are inhibited and the part performs an internal reset. If an access was in progress when the power supply fails, it will be automatically aborted by the FM24C16. When power rises back above 4.5V, a *start* signal must be issued by the bus master to initiate an access.

Slave Address

Following a *start*, the FM24C16 will expect a slave address byte to appear on the bus. This byte consists of three parts as shown in Figure 4.

- Bits 7 through 4 are the device type identifier which must be binary 1010 as shown.
- Bits 1 through 3 are the page select bits. They select which 256-byte block of memory will be accessed by this operation.
- Bit 0 is the read/write bit. If set to a 1, a read operation is being performed by the master; otherwise, a write is intended.

Word Address

After a slave device *acknowledges* the slave address on a write operation, the master will place the word address on the bus. This byte, in addition to the three page select bits from the slave address byte, forms the address of the byte within the memory that is to be written. This 11-bit value is latched in the internal address latch. There is no word address specified during a read operation, although the upper three bits of the internal latch are set to the page select values in the slave address.

During the transmission of each data byte and before the acknowledge cycle, the address in the internal latch is incremented to allow the following byte to be accessed immediately. When the last byte in the memory is accessed (at address hex 7FF), the address is reset to 0. There is no alignment requirement for the first byte of a block cycle — any address may be specified. There is also no limit to the number of bytes that may be accessed in a single read or write operation.

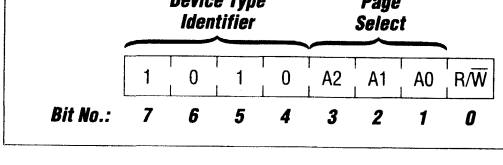
Data Transfer

After all address bytes have been transmitted, data will be transferred between the FM24C16 and the bus master. In the case of a read, the FM24C16 will place each of the eight bits on the bus and then wait for an acknowledge from the bus master before performing a read on the subsequent address. For a write operation, the FM24C16 will accept eight bits from the bus master and then drive the acknowledge on the bus.

All data and address bytes are transmitted most significant bit (bit 7) first.

After the acknowledge of a data byte transfer, the bus master may either begin another read or write on the subsequent byte, issue a *stop* command to terminate the block operation, or issue a *start* command to terminate the current operation and start a new one.

Figure 4. Slave Address



Write Operations

All write operations start with a slave and word address transmission to the FM24C16. In the slave address, bit 0 should be set to a 0 to denote a write operation. After they are acknowledged, the bus master transmits each data byte(s) to the FM24C16. After each byte, the FM24C16 will generate an acknowledge signal. Any number of bytes may be written in a single write sequence. After the last byte in the memory (address hex 7FF) is written, the address counter wraps around to zero so that the subsequent byte written will be the first (address 0).

There is no write delay on the FM24C16. Any operation, either a read or write to some other address, may immediately follow a write. Acknowledge polling, a sequence used with EEPROM devices to let the bus master know when a write cycle is complete, will return done immediately (the FM24C16 will acknowledge the first correct slave address).

If a write cycle must be aborted (with a *start* or *stop* condition), this should take place *before* the transmission of the eighth bit in order that the memory not be altered.

The write protect (WP) pin on the FM24C16 allows the upper half of the memory array (addresses hex 400 through 7FF) to be protected against accidental modification. When the pin is tied to V_{CC}, slave and word addresses targeted at the FM24C16 will still be acknowledged, but no acknowledge will occur on the data cycle if the address is in the upper half. In addition, no address incrementing occurs when writes are attempted to this half of the memory. If the write protection feature is not desired, this pin must be tied to V_{SS}.

Figure 5. Byte Write

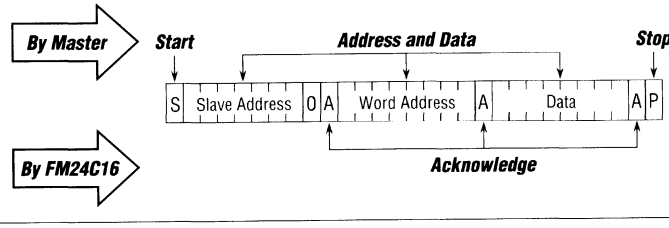
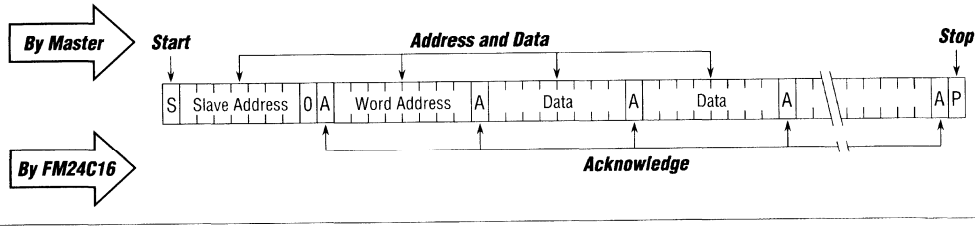


Figure 6. Multiple Byte Write



Read Operations

Current Address or Sequential Read

Sequential read operations take place from the address currently held in the internal address latch, and so require only that the bus master provide a slave address transfer before the FM24C16 begins the transfer of data to the master. In this slave address, bit 0 should be set to a 1 to denote a read operation. Note that the most significant three bits of the 11-bit internal address latch are specified by the slave address word, and are therefore *always* set during a read, regardless of which page the previous access referenced.

One or multiple bytes may be read from the FM24C16 in a single read operation. After the final byte has been read, the bus master signifies the end of the read sequence by failing to issue an acknowledge, or issuing a *stop* or *start* command. After the last byte in the memory (address hex 7FF) is read, the address counter wraps around to zero so that the subsequent byte to be read will be the first location in the memory (address 0). These sequences are shown below in Figures 7 and 8.

Selective (Random) Read

Selective, or random, read operations are possible on the FM24C16 by using the first two bytes of the *write* operation to load the internal address. The slave address for the part is sent out with bit 0 ($R/\overline{W}$) set to 0 to denote a write operation, and the word address is set to specify the least significant 8 bits of the desired address.

After the FM24C16 acknowledges this word address, the bus master should abort the *write* and begin the read with a *start* command. A new slave address is then sent out, this time with the $R/\overline{W}$ bit set to 1. Following the slave address and acknowledge, the FM24C16 will immediately begin transmission of the requested data. Figure 9 shows this operation.

Figure 7. Current Address Read

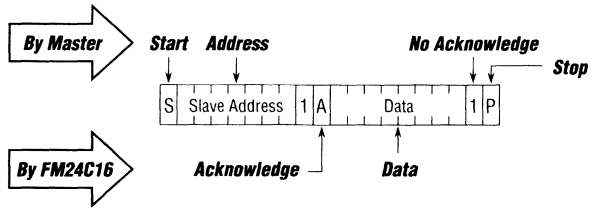


Figure 8. Sequential Read

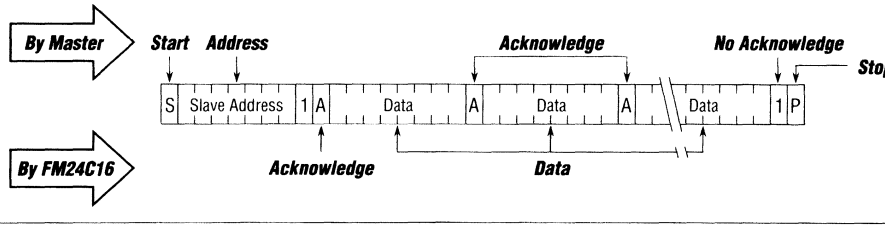
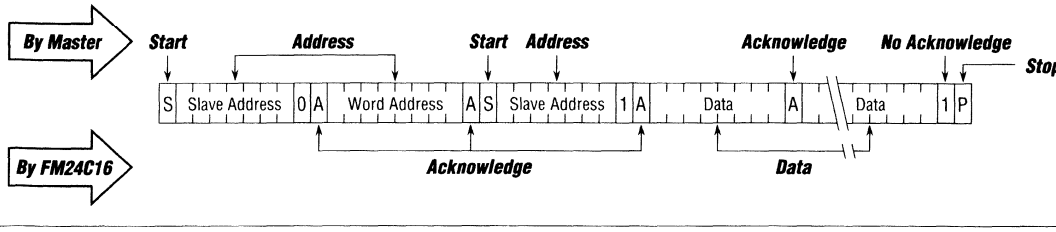
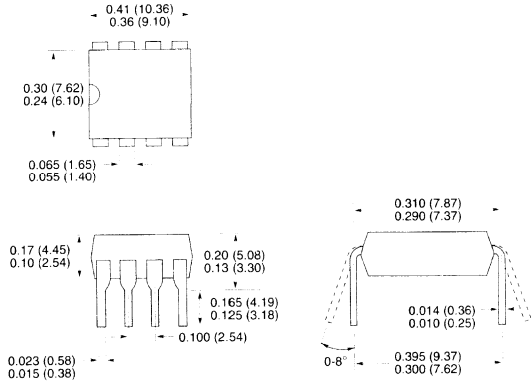


Figure 9. Selective Read

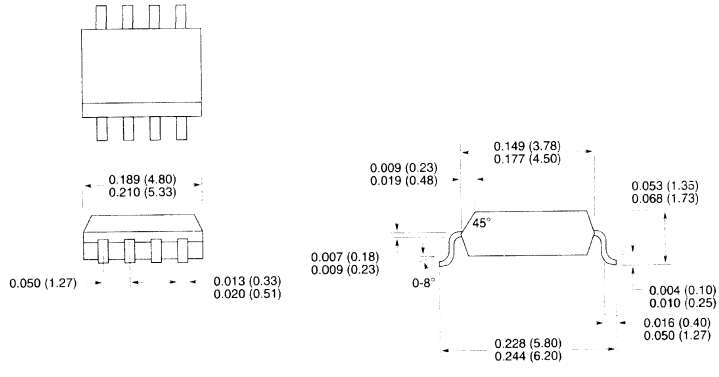


Packaging Information

8-Pin Plastic or Ceramic DIP



8-Pin SO (JEDEC)



Ordering Information

FM 24C16 - PS

Package Type (8-Pin)
PS - Plastic Skinny DIP
PT - Thin Plastic Skinny DIP
S - Plastic SOP
C - CERDIP

16K Serial FRAM Memory

Ramtron Ferroelectric Memory

THE FRAM TECHNOLOGY

1

Ramtron is the first semiconductor company to make the combined breakthroughs necessary in materials, processing, and design to manufacture solid state ferroelectric memory devices. The result of these achievements is a process which merges ferroelectrics with silicon to create ferroelectric random access memories (FRAM memories) with significant benefits compared to existing products.

The ferroelectric effect is the ability of a material to retain an electric polarization in the absence of an applied electric field. This stable polarization results from the alignment of internal dipoles within the Perovskite crystal units in the ferroelectric material. Application of an electric field that exceeds the coercive field of the material will cause this alignment, while reversal of the field reverses the alignment of these internal dipoles.

The name *ferroelectric* derives from the similarity to a ferromagnetic material's ability to exhibit a magnetic polarization in the absence of an applied magnetic field. Ferroelectric materials are insensitive to magnetic fields. The construction of the FRAM memory products also makes them insensitive to practical external electric fields.

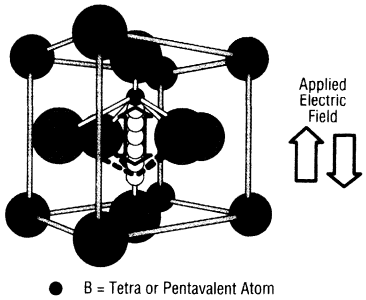


Fig. 1 **Perovskite Crystal Unit Cell**

A simplified model of a unit ferroelectric crystal is shown in Figure 1. An externally applied electric field will move the center atom into one of the two stable positions shown based upon the direction of the field. Once the external field is removed, the atom remains in a stable position. Since no external electric field or current is required for the ferroelectric material to remain polarized in either state, a memory device can be built for storing digital (binary) data that will not require power to retain information stored within it.

By applying the interdisciplinary talents of its staff, Ramtron has developed a complex proprietary thin-film ferroelectric material which is compatible with standard semiconductor fabrication techniques. The nonvolatile storage element in FRAM memories is a capacitor constructed from two metal electrodes and a ferroelectric thin film inserted between the transistor and metallization layers of a CMOS process.

Data stored in a ferroelectric memory cell can be read by applying an electric field to the capacitor. If the applied field is in the direction to switch the internal dipoles, more charge will be moved than if the dipoles are not reversed. Sense amplifiers built into the FRAM chips measure this charge and produce either a zero or one on the output pins. After the read takes place, the chip automatically restores the correct data to the cell.

Another aspect of the Ramtron ferroelectric material — its very high dielectric constant — permits the very efficient construction of capacitor elements on the chip. For use as both data storage, such as in a DRAM cell, or power storage, such as on a remotely accessed system, this property of the material offers the potential for a wide variety of new devices.

The development of the FRAM memory has required significant effort from a combined team of highly trained engineers and scientists and is covered under numerous patents. As these development efforts continue, the capabilities of the chips built by Ramtron will continue to increase and their cost will decrease. Using advanced ferroelectric technology, in the future Ramtron will be able to approach the density and manufacturing economics of DRAM memory, providing the ideal memory solution for almost every application.

(Continued on Back)

Ferroelectric random access memories (FRAM memories) from Ramtron combine the features of several different types of memory to offer a true system memory solution. They integrate the fast reads and writes of SRAM, the nonvolatility of EEPROM, and very high read/write endurance onto a single, cost effective chip.

Current FRAM products are built using a dual element differential sense approach, as shown in Figure 1. In this architecture, somewhat like an SRAM cell, two nonvolatile elements are integrated in every memory cell, each polarized in the opposite direction. To read the state of the memory cell, both nonvolatile elements are polarized in the same direction. A differential amplifier (sense amp) connected to the bit lines measures the difference between the amount of charge transferred from the two cells and sets the output accordingly.

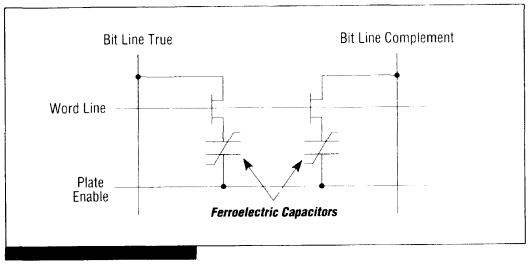


Fig. 1 **Dual Memory Element Cell**

Differential cells are inherently reliable since common mode variations in the characteristics of the nonvolatile elements are canceled out. Unfortunately, they require two nonvolatile elements, two access devices, and two bit lines. In order to increase the density of the FRAM devices, future Ramtron designs will employ single cell architectures that use only one nonvolatile element in each cell.

A single ended FRAM cell is shown in Figure 2. In this architecture, which is similar to that of a standard DRAM or EEPROM, only one nonvolatile element is used. When reading the cell, the element is polarized and the charge transferred is compared to a reference cell or other fixed level. The result of this comparison determines whether a one or a zero was stored in the cell.

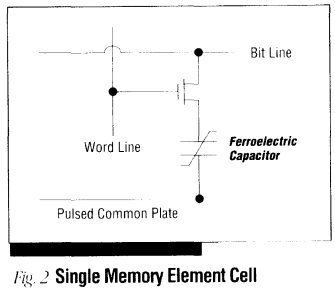


Fig. 2 **Single Memory Element Cell**

Like a DRAM, all FRAM accesses modify the state of the storage element, which is then internally restored by the chip during the precharge portion of the cycle. This operation takes place automatically, without any intervention from the system.

Two key aspects of the FRAM technology allow Ramtron to offer products that are superior to those manufactured with other EEPROM technologies. First, it employs a polarization technique instead of a charge tunneling mechanism. Second, it permits all internal operations to utilize five volts, instead of the 12 to 15 volts required by conventional EEPROM technologies.

In order to program (write) a state into a FRAM cell, the electric field need be applied for less than 100ns in order to polarize the nonvolatile elements. In a standard EEPROM, it takes a millisecond or more for sufficient charge to travel through the insulating oxides to charge up the gate element. In addition, the high voltage generation circuitry takes some time to stabilize before it can cause this transfer to take place. These differences allow a FRAM memory cycle time of 500ns worst case, compared to 10ms for an EEPROM.

In an EEPROM, the charge tunneling across the oxide layer degrades its characteristics of the oxide, causing catastrophic breakdown or excessive trapped charge. For these reasons, EEPROM devices are guaranteed for only 10,000 to 100,000 write cycles. FRAM memories do not suffer from these same limitations, and so can provide 10 billion (10^{10}) cycles, although both read and write operations must adhere to these limits.

High voltage generation requires an oscillator, charge pump, charge storage capacitor, and regulator circuit on the chip, which take significant area on an EEPROM. In addition, this added circuitry increases the power consumption of the chip, which can be quite significant for some products. For example, the FM24C04 serial 4K FRAM memory uses 10 to 50 times less active power than competing parts.

Connecting high voltages to the individual cells requires that critical layout dimensions within the memory array be larger to withstand the increased voltage levels. While current FRAM products utilize 1.5µ and 1.2µ rules to simplify fabrication, future products will be able to take advantage of the latest CMOS technologies to achieve the high density and low cost typical of DRAMs.

Benefits Of Ramtron's FM24C04 Serial FRAM® Memory

Application Brief

1

Ramtron's FM24C04 serial ferroelectric random access memory, or FRAM™ memory, is completely plug compatible with I²C based 24C04 parts manufactured by Xicor, Signetics, Microchip, SGS Thomson, Atmel, and others, but provides C.L.E.A.R. advantages. The bar graphs in Figure 1 graphically show some of these benefits.

Serial access parts are often used in microcontroller based products. As such applications often do not demand fast access or high density, the low cost of the FM24C04 can provide a significant savings. In a system with no other external memory, adding a parallel access EEPROM requires as many as 19 I/O pins to be used, while the FM24C04 requires only two pins. Since the part only has eight pins, it can be fit into a 5mm x 6mm SOP package, requiring very little board space.

Ramtron's FRAM memory is based on thin film ferroelectric storage elements developed and patented by Ramtron. This architecture provides random access, but all writes are nonvolatile so there are no long 10ms delays.

Since there is no write delay, there is no need for the processor to perform an acknowledge polling loop to determine whether the serial part is available. If an acknowledge poll cycle is initiated in a system containing the FM24C04, it will immediately acknowledge that any previous write has completed.

Another advantage of the immediate write is that the entire memory can be written with a single page mode cycle. For conventional serial EEPROMs, only 16 bytes can be written, after which the processor must wait for the internal write of 10ms to complete before issuing another page mode cycle.

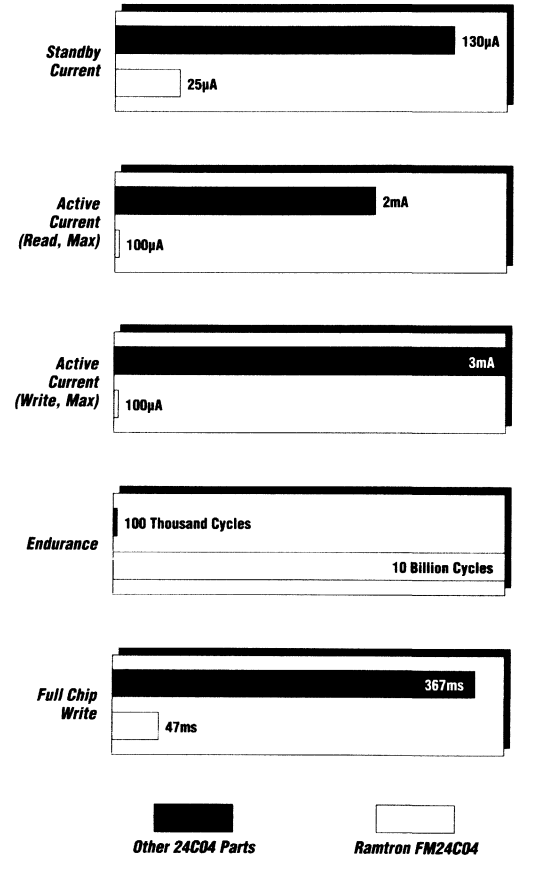
Both the active and standby current consumption of the Ramtron part is significantly lower than other manufacturers. Typical CMOS standby current for the FM24C04 is only 10µA, which can greatly extend operating life in battery powered systems, compared to other serial EEPROMs which take up to 750µA. Active current is only 100µA (maximum), versus 2mA or 3mA for other parts.

The high write endurance of the FM24C04 provides for longer system life in any write intensive application. At 10 billion read/write cycles, it is 10,000 to 100,000 times greater than any other serial EEPROM, allowing more efficient usage.

Write protection for the upper 256 bytes of memory can be obtained by connecting the WP pin to V_{CC}. This feature allows the designer to use this block for information such as a serial number or calibration data which is entered into the memory when the system is built. During normal operation of the system, no changes can occur in this block of memory.

The FM24C04 is available in an 8-pin mini-DIP as well as an 8-pin SOP package, ideal for space limited applications.

Figure 1. FRAM Benefits



Endurance Considerations For FRAM® Memory

Application Brief

1

Ramtron's ferroelectric random access memory (FRAM memory) devices, like most other nonvolatile storage devices, allow a limited number of write operations to take place over the life of the part. This limit, known as the endurance of the device, also applies to read operations on a FRAM memory. This applications brief explains the endurance requirements for various system environments.

Traditional EEPROM devices usually have write cycle limitations of between 10,000 (10^4) and 100,000 (10^5) cycles. They have no limitations on the number of reads that may be performed. In contrast, FRAM memories have an endurance rating of 10 billion (10^{10}) cycles, but this limit applies to read operations as well as writes.

FRAM memories utilize a thin film ferroelectric material to form the nonvolatile element, polarizing it in one direction or another in order to store a binary value. EEPROMs rely on charge tunneling through an oxide to a floating gate, resulting in higher material stresses and lower endurance. Other benefits of the technology include very fast write cycle times (340ns to 400ns instead of 10ms), completely random access (no page mode organization), and true 5V only operation within the device.

In many applications requiring nonvolatile memory, a single byte or group of bytes are written frequently, perhaps to update the current state of the system or to keep track of the current time. In such situations, the rate at which these updates take place, along with the lifetime of the system, determines the endurance requirement for the nonvolatile memory.

Table 1 lists the nonvolatile memory endurance requirements for a number of different situations. It shows that writes at intervals between 30 milliseconds (33Hz) and one hour cannot be satisfied with an EEPROM, but work quite well with the FRAM memory.

Table 1 assumes system operation 24 hours per day, 365 days per year. For many systems, such as consumer electronics, vending machines, or cellular phones, this assumption may result in excessive endurance requirements. Entries in the table should be reduced appropriately for these applications.

Program store applications are generally considered to require very high read endurance, since even slow processors execute instructions (and therefore read them from memory) at 1µs intervals. The first line in Table 1 below includes the (read) endurance required for a simple program loop that is assumed to consist of a 10-byte program executed at 1µs per instruction.

For interrupt or other asynchronous event handling, however, the endurance requirements for program storage could be much lower. To cite a simple example, a system might maintain the current time of day by interrupting the processor every second. That interrupt handler would require only a 10^9 endurance level.

Another important application area is continuous data storage. Example systems might include data acquisition systems, such as test and measurement equipment or flight data recorders, and first-in/first-out (FIFO) buffers, such as disk write buffers or some high reliability network systems. In these applications, the memory is usually organized as a circular buffer.

Table 1. Endurance Requirements

ACCESS FREQUENCY		PRODUCT LIFETIME			APPLICATION
Interval	Rate	5 Year	10 Year	15 Year	
10µs	100KHz	10^{14}	10^{14}	10^{14}	Program Loop
23µs	44KHz	10^{13}	10^{13}	10^{14}	Digital Audio
1ms	1KHz	10^{12}	10^{12}	10^{12}	
17ms	60Hz	10^{10}	10^{11}	10^{11}	Line Frequency
30ms	33Hz	10^{10}	10^{10}	10^{11}	1800 RPM
50ms	20Hz	10^{10}	10^{10}	10^{10}	
1 Second	1Hz	10^9	10^9	10^9	Simple Clock
3 Seconds		10^8	10^8	10^9	
1 Minute		10^7	10^7	10^7	
15 Minutes	96/Day	10^6	10^6	10^6	Frequent Usage
1 Hour	24/Day	10^5	10^6	10^6	
8 Hours	3/Day	10^4	10^5	10^5	Normal On/Off

In a circular buffer, the memory is accessed sequentially using pointers or key memory values to locate the current head or tail of the list, which constantly cycle through the array. If the system contains more than one FRAM device, all locations in the first device would be accessed, followed by each of the other devices in a serial manner. For a system with this type of architecture, the endurance requirement depends on both the access rate and the depth of the buffer.

Table 2 below shows the endurance requirements for various buffer depths. Since bandwidth is a key parameter for such systems, that number is also listed in the table below. The bandwidth numbers shown in this table are in *bytes* per second, not bits per second, for 1- and 4-byte buffer widths. All values in the table assume a ten year product life.

In summary, an understanding of the application is required to determine the endurance necessary for nonvolatile memory. Systems which require writes to occur at a rate faster than once per hour for 10 years would benefit from the high endurance capabilities of FRAM memory.

Table 2. Endurance Requirements

ACCESS FREQUENCY		ENDURANCE				BANDWIDTH	
Interval	Rate	Buffer Depth				Buffer Width	
		512	8K	64K	256K	1 Byte	4 Bytes
100ns	10MHz	10^{13}	10^{12}	10^{11}	10^{10}	10M	40M
1µs	1MHz	10^{12}	10^{11}	10^{10}	10^{9}	1M	4M
10µs	100KHz	10^{11}	10^{10}	10^{9}	10^{8}	100K	400K
100µs	10KHz	10^{10}	10^{9}	10^{8}	10^{7}	10K	40K
1ms	1KHz	10^{9}	10^{8}	10^{7}	10^{6}	1K	4K

Replacing A Dallas Semiconductor DS1225 With FRAM® Memory

Application Note

1

Ramtron's FM1608S 8k x 8 ferroelectric random access memory (FRAM memory) provides an ideal replacement for many integrated battery-backed SRAM (BBSRAM) products such as Dallas Semiconductor's DS1225 or SGS/Thomson's MK48Z09.

FRAM memories are monolithic nonvolatile chips based on ferroelectric technology. They feature fast write cycles and high read/write endurance in standard surface mount and DIP packaging in 512 x 8 and 8k x 8 densities.

In many application scenarios, such as storing critical information after a power loss, continuous storage of diagnostic data, current equipment, or supply status, user programming, factory calibration/configuration, or up-to-date machine status, a FRAM memory offers significant benefits compared to a BBSRAM.

- ***Reduced Component Size*** — BBSRAM products are only available in high (0.4 inch) 600 mil packages. FM1608S devices are available in the standard surface mount package. In addition, they are available in DIP packages with the same footprint and pinout as the BBSRAM products.
- ***Cost*** — Because they contain an SRAM, lithium battery, and power management chip, the cost of a BBSRAM plus the added manufacturing cost is substantially higher than a Ramtron FM1608S.
- ***Ease of Manufacture*** — Because the FM1608S is packaged in standard profile plastic DIP and surface mount packages, it can be assembled on the PC board with all other components. BBSRAM products are typically hand inserted or socketed.
- ***Product Lifetime*** — Although specified as 10 years at room temperature (25°C), battery-backed devices will exhibit significantly shorter life if exposed to elevated temperature or frequent power transitions. When a BBSRAM fails, the product must be returned to the factory to have the system repaired. The FM1608S has a retention specification of 10 years but can be reprogrammed after 10 years if necessary for an arbitrarily long lifetime. There is no way to determine the life remaining in such a battery.
- ***Current Consumption*** — The DS1225 BBSRAM draws 75mA when active and 5ma while in standby mode. The FM1608S draws 25mA when active and only 100µA when in standby mode. For small battery-powered systems, this difference can significantly increase battery life.
- ***Design Sensitivity*** — The power-up/power-down ramp rates affect reliability and product life for BBSRAMs, as specified in their datasheets. A FRAM memory has no such requirement. BBSRAM products are also much more sensitive to over voltage and under voltage conditions on their pins, situations which can easily occur during brown outs or power failures.

Replacing a BBSRAM with an EEPROM is usually impossible. EEPROMs have limited write endurance, typically 10,000 to 100,000 cycles, so writes must be managed carefully by the system. EEPROMs also have long write delays after a write cycle, often up to 10ms, requiring software delay loops. This extended write delay also makes it difficult to save data during an unexpected power loss.

A patented ferroelectric technology has allowed Ramtron's FRAM memory to offer these benefits without many of the disadvantages of EEPROMs. The fundamental nonvolatile write mechanism is based on a polarization principle, so it can be accomplished within the write cycle and does not require the long 10ms delay typical of EEPROMs. Since random writes can take place anywhere in the FRAM memory, there is no need to organize nonvolatile data within EEPROM pages to reduce delay time, a significant software benefit.

A second advantage of ferroelectric technology is substantially higher endurance — 10 billion read/write cycles, versus only 100,000 for EEPROMs. Note that with FRAM memory, both reads *and* writes cause a nonvolatile cell change to take place, so each require an endurance cycle.

With minor system changes, the FM1608S can replace a BBSRAM. Systems that function properly with a FRAM device will also work with a BBSRAM in the same socket. Designers should be aware of the following when modifying a system to accept the FRAM product:

1) The FM1608S has an internal address latch that is triggered by the falling edge of $\overline{CE}$. With a BBSRAM, addresses may change before or after chip enable is asserted — the access is re-started with every transition on the address lines.

Figure 1. Read Access

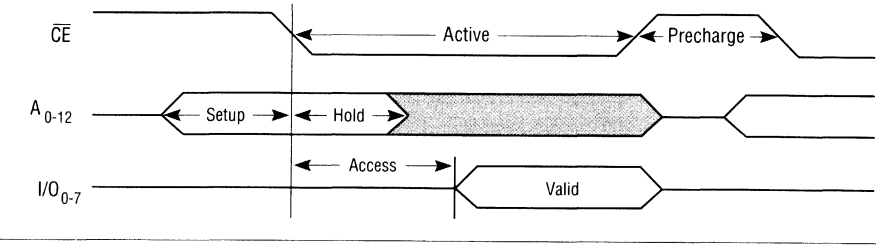


Figure 1 shows the basic timing required for a read access on the FM1608S.

2) Typically, the output of an address decoder is connected directly to the memory. In some systems, chip enable may be connected to ground, permanently enabling the RAM, with the output enable being connected to the decoder. Without minor circuit changes, neither of these two configurations will permit the FM1608S to operate properly.

3) In order to make the FM1608S operate properly, either a strobe from the processor (such as ALE or AS) or one of the processor clock signals can be used to gate the decoded addresses to generate a proper chip enable for the FM1608S. Figure 2 shows an example circuit for an Intel 80C51 family processor. The 74HCT373 latch is not necessary for proper operation, as port 0 may be directly connected to the lower address pins on the FRAM.

4) Note that an access takes place within the FM1608S when chip enable is asserted regardless of the state of output enable ($\overline{OE}$). If $\overline{OE}$ is used as a second chip select during read operations, then additional circuitry must be placed in the chip enable path to prevent the access if it is not to that particular FRAM.

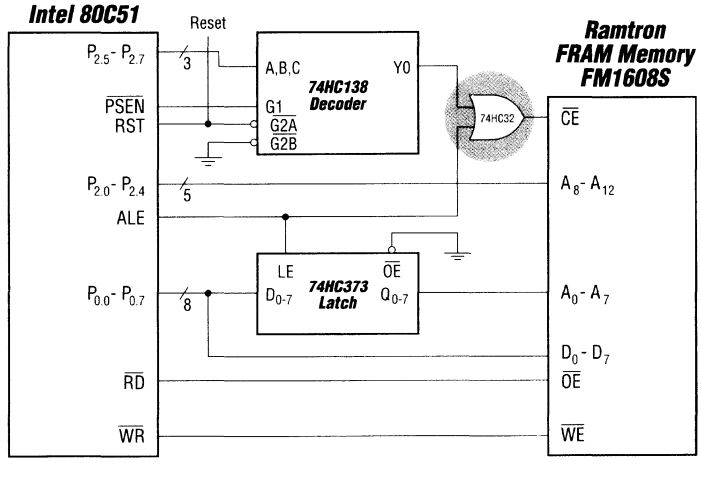
5) The access time of the FM1608S is 250ns for both reads and writes. Systems which require the faster 150 or 170ns access time of the Dallas part will have to add extra wait states to accommodate the Ramtron part.

6) The FM1608S specifies a precharge time of 140ns. This is the time after an access has terminated (chip select goes high) before which another access can take place. In most situations, the processor and related control circuitry will provide this delay without additional circuitry. There is no precharge requirement for BBSRAMs.

7) Read endurance (plus write endurance) is limited (on the FRAM memory to 10 billion cycles. For this reason, constant program execution cannot take place directly out of the FRAM memory. For a system in full operation 24 hours per day, 265 days per year, accesses to a particular location may take place at a rate of about every three seconds for a 10 year product life. Of course, for systems that do not see continuous usage, accesses may take place at a greater frequency.

In most applications, Ramtron's FM1608S offers reduced board space, increased reliability, enhanced performance and lower cost compared to integrated battery backed SRAM products.

Figure 2.



RAMTRON

EDRAM Memory Products

2

DM2200 EDRAM
4Mb x 1 Enhanced Dynamic RAM

Product Specification

Features

- 2Kbit SRAM Cache Memory for 15ns Random Reads Within a Page
- 8ns Burst Read Capability
- Fast 4Mbit DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- Simple On-chip Page Caching Control Allows DRAM-like System Architecture and Compatibility
- 256-byte Wide DRAM to SRAM Bus for 7.3 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintains Cache Coherency on Writes
- Hidden Precharge Cycles
- Hidden Refresh or /CAS Before /RAS Type Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- 300 Mil Plastic SOJ Package

Description

The Ramtron 4Mb enhanced DRAM combines raw speed with innovative architecture to offer the optimum cost-performance solution for high performance local or system main memory. In most high speed applications, no-wait-state performance can be achieved without secondary SRAM cache and without interleaving main memory banks at system clock speeds of greater than 66MHz. The EDRAM outperforms conventional SRAM cache plus DRAM memory systems by minimizing processor wait states for all possible bus events, not just cache hits. The combination of input data and address latching, 2K of fast on-chip SRAM cache, and simplified on-chip cache control allows system level flexibility, performance, and overall memory cost reduction not available with any other high density memory component. Architectural similarity with JEDEC DRAMs allows a single memory controller design to support either slow JEDEC DRAMs or high speed EDRAMs. A system designed in this manner can provide a simple upgrade path to higher system performance.

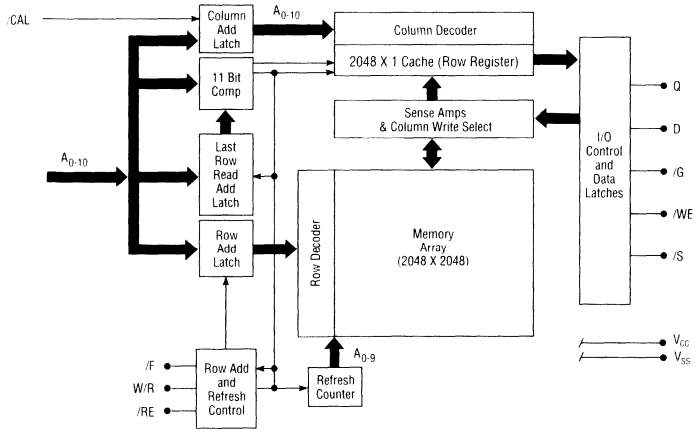
Architecture

The architecture is similar to a standard 4Mb page mode or static column DRAM with the addition of an integrated cache and internal control which allows it to operate much like a page mode or static column DRAM.

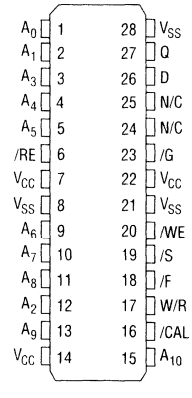
The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the internal comparator detects a page hit, only the SRAM is accessed and data is available in 15ns from column address. When a page read miss is detected, the new DRAM row is loaded into the cache and data is available at the output all within 35ns from row enable. Subsequent reads within the page (burst reads or random reads) can continue at 15ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

2

Functional Diagram



Pin Configuration



Memory writes are internally posted in 15ns and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 15ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance without any significant increase in die size over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address changes. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	↓	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

write, write-verify, or random read-write sequences within the page with 15ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time t_{AC} after the column address is setup to /CAL.

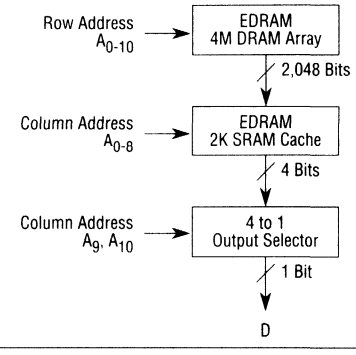
Function	/S	/G	/CAL	A_{0-10}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

On-Chip SRAM Interleave

The DM2200 has on-chip interleave of its SRAM cache which allows 8ns random accesses (t_{AC1}) to up to three data words (burst reads) following an initial read access (hit or miss). The SRAM cache is integrated into the DRAM array in a 512 x 4 organization. It is converted into a 2K x 1 page organization by using an on-chip address multiplexer to select one of four bits to the output pin D (as shown below). The specific databit selected to the output pin is determined by column addresses A_9 and A_{10}. System operation is consistent with the standard "Functional Description" and timing diagrams shown in this specification. See the note in the read timing diagrams and "Switching Characteristics" chart for the faster access and data hold times.

DM2200 Datapath Architecture



Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F type refresh cycle. When /F type refreshing is used, at least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled. In this case, the output remains disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization.

Unallowed Mode

Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. If these techniques are used, the EDRAM will require only four control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], W/R, and /G). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CAL — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pin during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition; read and write cycles cannot be executed while /S is high. /S must remain active throughout any read or write operation. Only the /F refresh operation can be executed when /S is high.

D — Data Input

This input pin is used to write data to the EDRAM.

Q — Data Output

This output pin is used to read data from the EDRAM.

$A_{0\text{-}10}$ — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 11-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

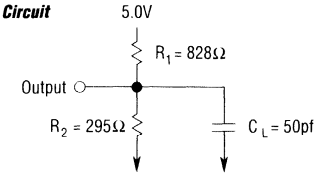
Pin Names

Pin Names	Function
A_0 - A_{10}	Address Inputs
/RE	Row Enable
D	Data In
Q	Data Out
/CAL	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V)

Pin Names	Function
V_{SS}	Ground
/WE	Write Enable
/G	Output Enable
/F	Refresh Control
/S	Chip Select - Active/Standby Control
N.C.	No Connection

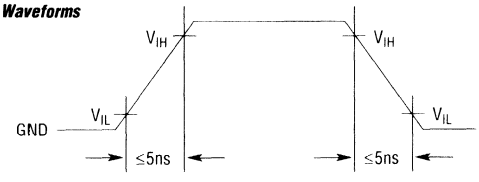
AC Test Load and Waveforms

Load Circuit



Input Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}



Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current (I_{OUT})	50mA*

*One output at a time; short duration.

Capacitance

Description	Max	Pins
Input Capacitance	7pf	A_0 - A_9
Input Capacitance	6pf	D
Input Capacitance	10pf	A_{10}, /CAL, /RE, W/R, /WE, /F, /S
Input Capacitance	2pf	/G
Output Capacitance	6pf	Q

Electrical Characteristics

(T_A = 0 - 70°C)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	-10µA	10µA	$0V \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-10µA	10µA	$0V \le V_{IN}$, $0V \le V_{OUT} \le 5.5V$

Symbol	Operating Current	33MHz Typ(1)	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	110mA	215mA	170mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	65mA	115mA	90mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	55mA	110mA	85mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	135mA	190mA	150mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	50mA	135mA	105mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	1mA	1mA	1mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	30mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. In this typical example, page mode and random reads refers to page burst hits and misses. Writes are two clock cycle random and page mode writes. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{AC}[1]	Column Address Access Time for Addresses A_{0-8}		15		20	ns
t_{AC1}[1]	Column Address Access Time for Addresses A_9 and A_{10}		8		9	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
t_{AQX}	Column Address Change to Output Data Invalid for Addresses A_{0-8}	5		5		ns
t_{AQX1}	Column Address Change to Output Data Invalid for Addresses A_9 and A_{10}	1		1		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		6		ns
t_C	Row Enable Cycle Time	65		85		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
t_{CA}	Address Cycle Time (Cache Hits)	15		20		ns
t_{CAE}	Column Address Latch Active Time	6		7		ns
t_{CAH}	Column Address Hold Time	0		1		ns
t_{CDR}[2]	Column Address Delay from /RE Low, After /CAL Assertion in a Write Hit Cycle	35		45		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		7		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-1		-1		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		17		20	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid for Addresses A_{0-8}	5		5		ns
t_{CQX1}	Column Address Latch Inactive to Data Invalid for Addresses A_9 and A_{10}	1		1		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		6		ns
t_{CWL}	/WE Low to /CAL Inactive	5		7		ns
t_{DH}	Data Input Hold Time	0		1		ns
t_{DS}	Data Input Setup Time	5		6		ns
t_{GQV}[1]	Output Enable Access Time		5		6	ns
t_{GQX}[3,4]	Output Enable to Output Drive Time	0	5	0	6	ns
t_{GQZ}[5,6]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	6	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		1		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		6		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
t_{PC}	Column Address Latch Cycle Time	15		20		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		35		45	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		17		22	ns
t_{RAC2}[1,7]	Row Enable Access Time for a Cache Write Hit		35		45	ns
t_{RAH}	Row Address Hold Time	1.5		2		ns

Switching Characteristics (continued)

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{RE}	Row Enable Active Time	35	100000	45	100000	ns
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	10		13		ns
t_{RP}(8)	Row Precharge Time	25		32		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		1		ns
t_{RSH}	Last Write Address Latch to End of Write	15		20		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	40		51		ns
t_{RWL}	Last Write Enable to End of Write	15		20		ns
t_{SC}	Column Address Cycle Time	15		20		ns
t_{SHR}	Select Hold From Row Enable	0		1		ns
t_{SQV}(1)	Chip Select Access Time		15		20	ns
t_{SQX}(3,4)	Output Turn-On From Select Low	0	15	0	20	ns
t_{SQZ}(5,6)	Output Turn-Off From Chip Select	0	10	0	13	ns
t_{SSR}	Select Setup Time to Row Enable	5		6		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	15		20		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
t_{WHR}	Write Enable Hold After /RE	0		1		ns
t_{WI}	Write Enable Inactive Time	5		7		ns
t_{WP}	Write Enable Active Time	5		7		ns
t_{WQV}(1)	Data Valid From Write Enable High		15		20	ns
t_{WQX}(3,6)	Data Output Turn-On From Write Enable High	0	15	0	20	ns
t_{WQZ}(4,5)	Data Turn-Off From Write Enable Low	0	15	0	20	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Cache Miss)		15		20	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Column Address Ignored Prior to t_{CDR} for This Specific Cycle

(3) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and Not Referenced to V_{OH} or V_{OL}

(4) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

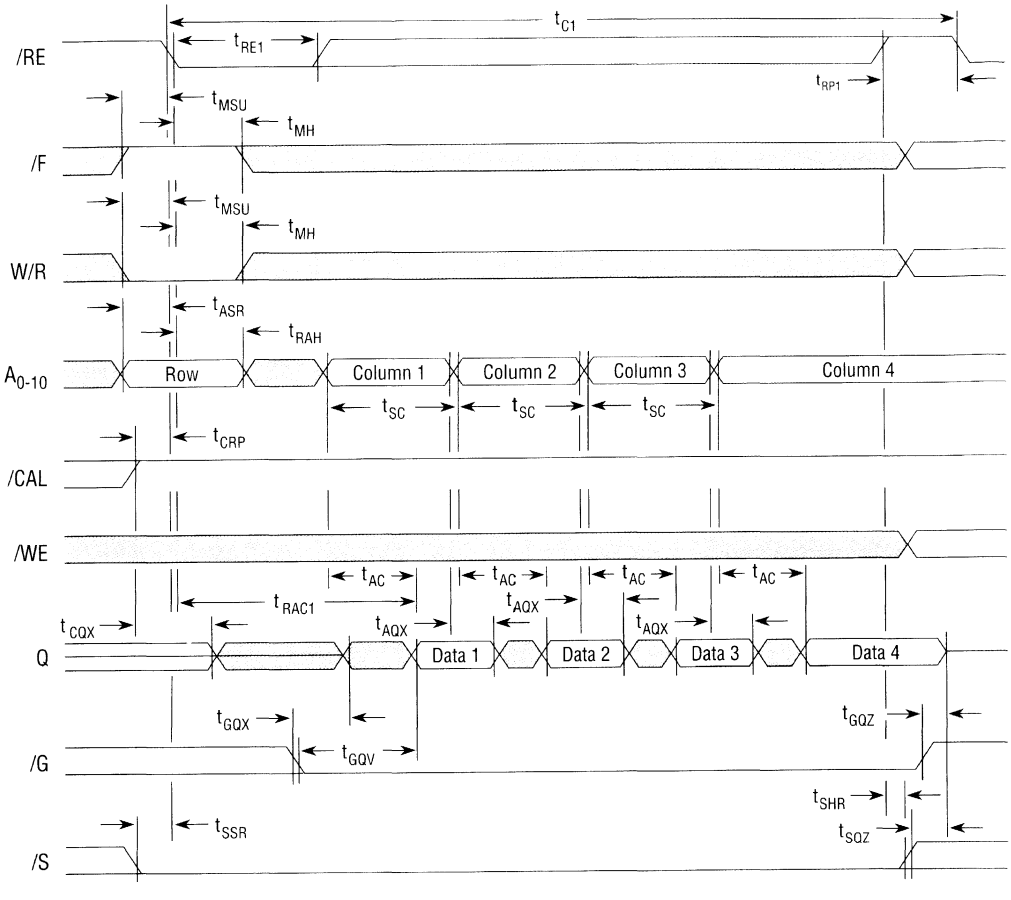
(5) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

(6) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(7) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

(8) For Back-to-Back /F Refreshes, t_{RP}=40ns. For Non-consecutive /F Refreshes, t_{RP}=25ns and 32ns Respectively

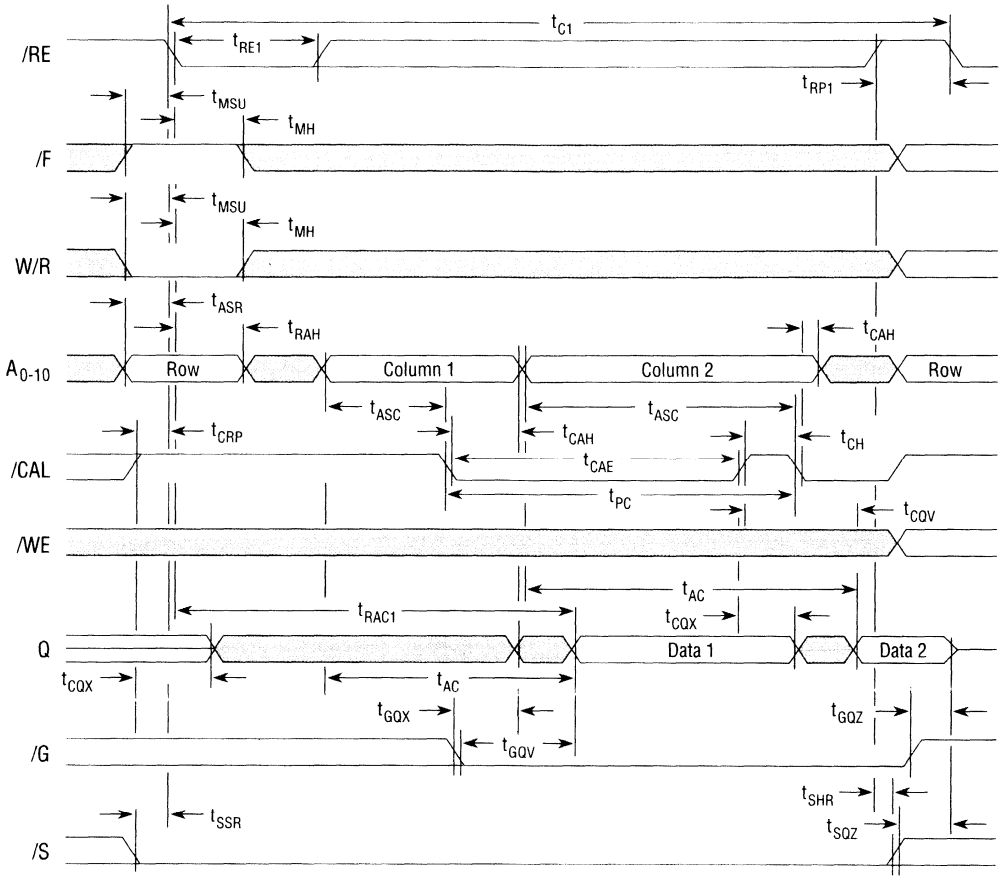
/RE Active Cache Read Hit (Static Column Mode)



Don't Care or Indeterminate ☐

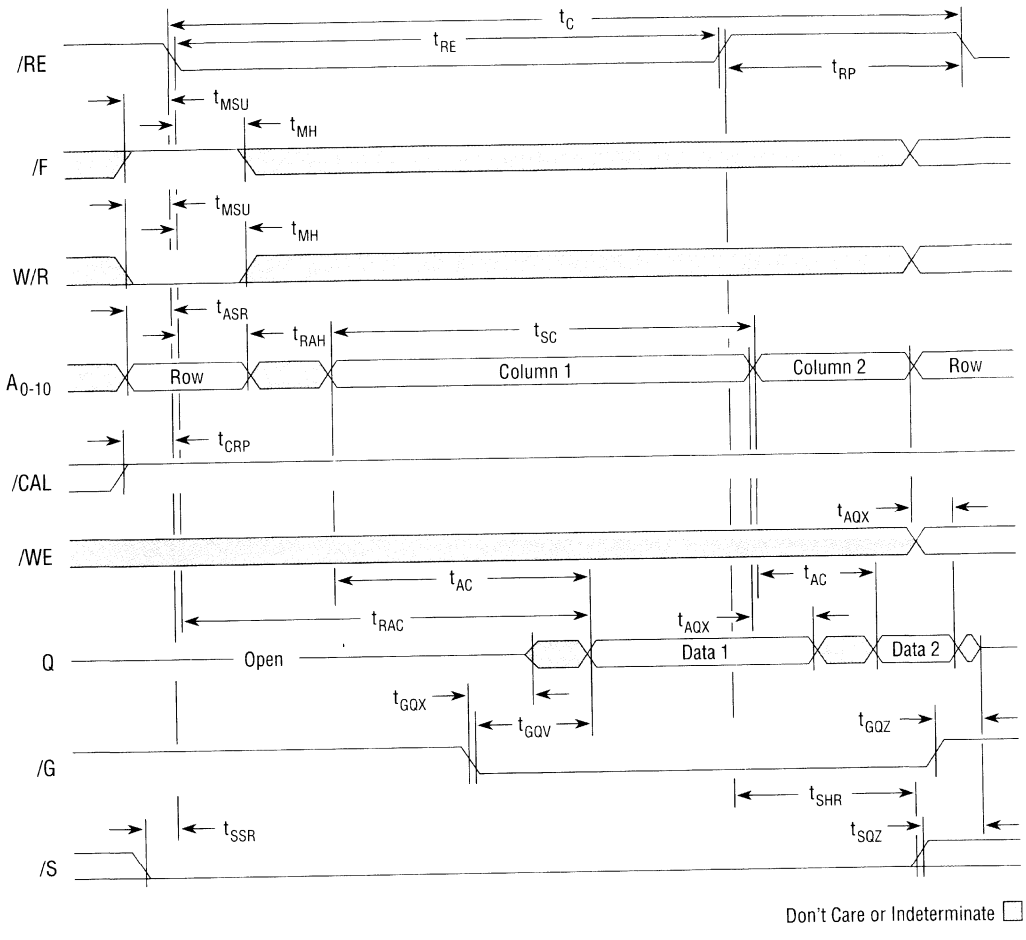
NOTES: 1. If column address 2, 3, or 4 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{ACI} for data 2, 3, and 4, and t_{AQX} becomes t_{AQXI} for data 1, 2, and 3.

/RE Active Cache Read Hit (Page Mode)



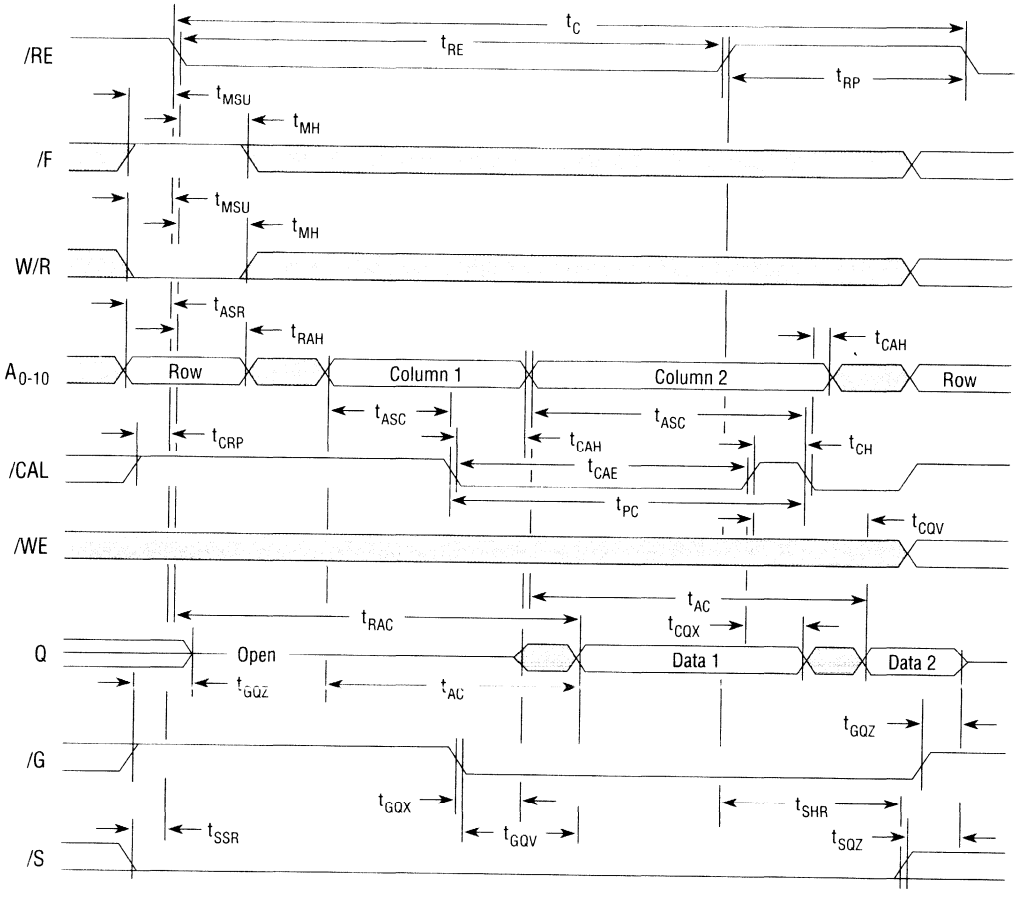
NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, and t_{CQX} becomes t_{CQX1} for data 1.

/RE Active Cache Read Miss (Static Column Mode)



NOTES: 1. If column address 2 modifies only address pin A_0 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, and t_{AQX} becomes t_{AQX1} for data 1.

/RE Active Cache Read Miss (Page Mode)

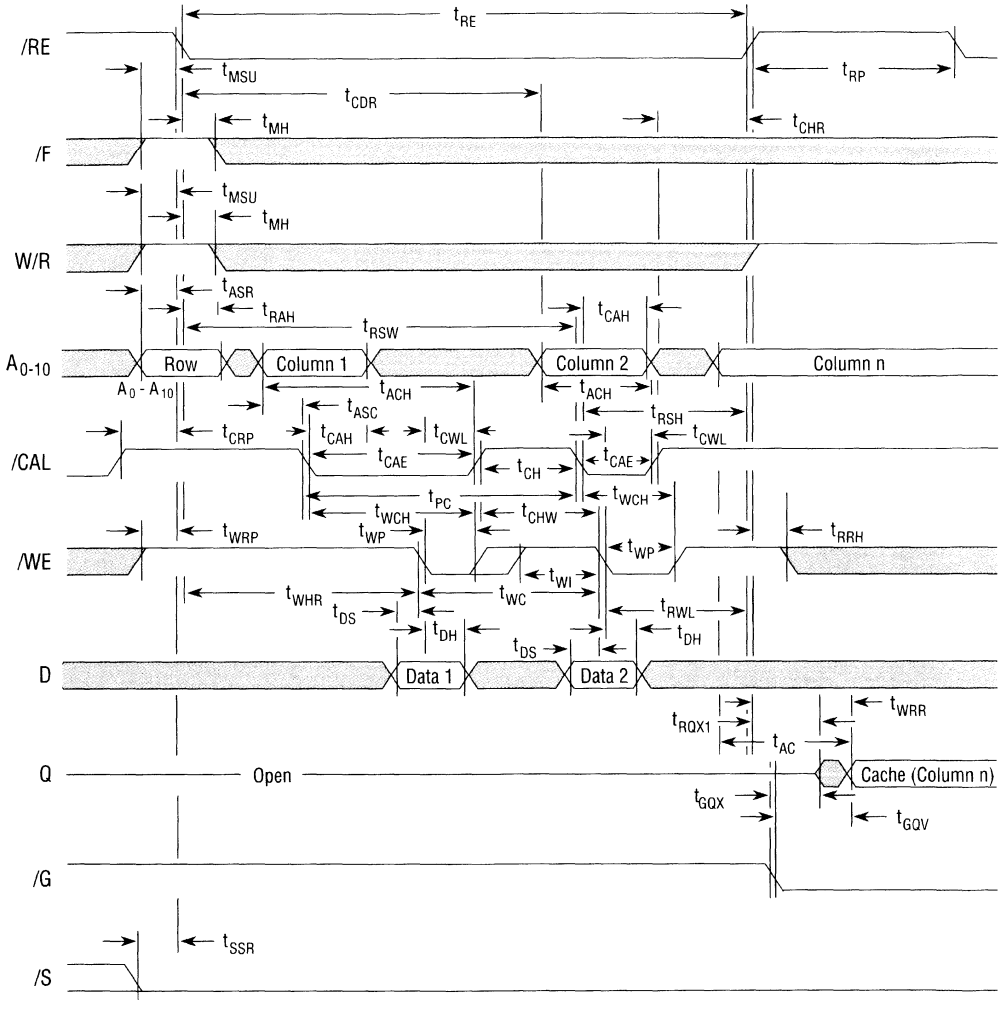


Don't Care or Indeterminate ☐

NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{ACI} for data 2, and t_{CQX} becomes t_{CQXI} for data 1.

2

Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



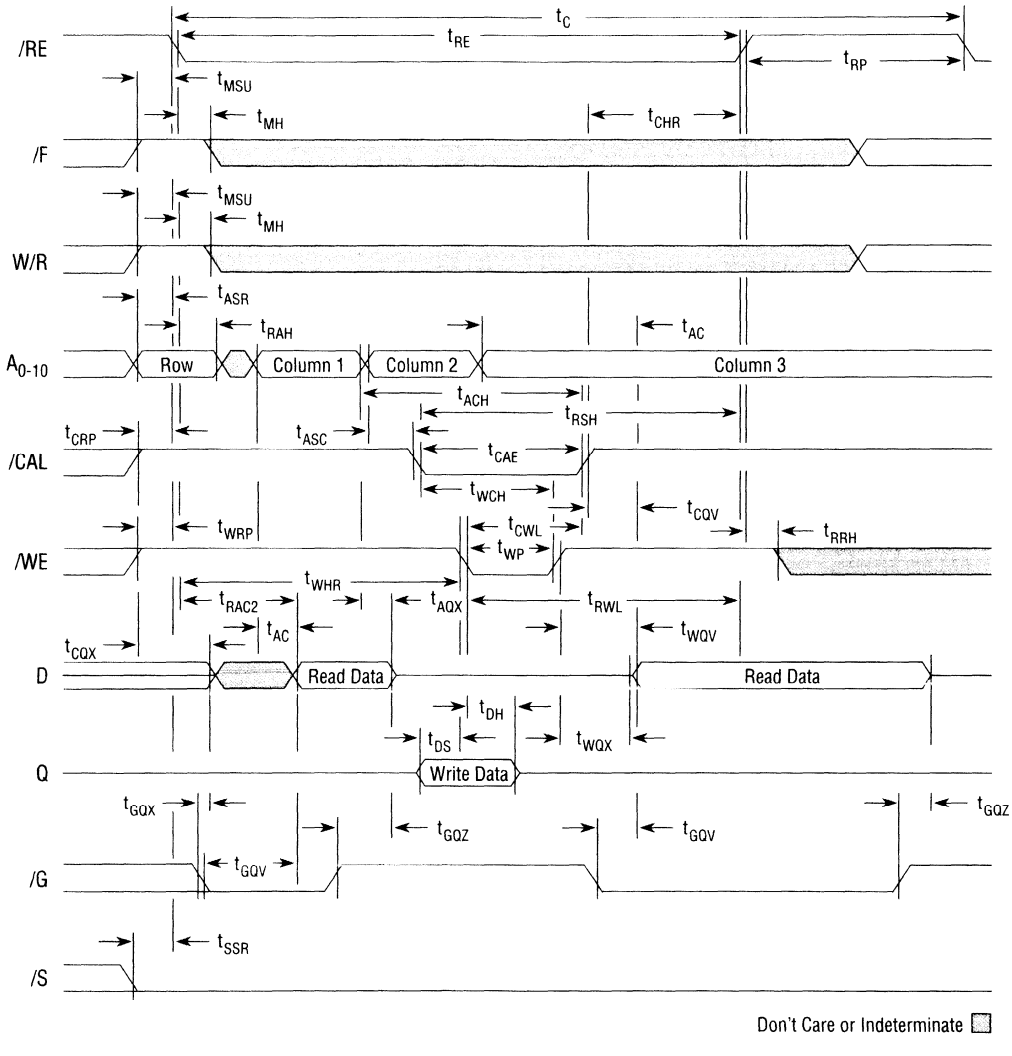
Don't Care or Indeterminate ☐

NOTES: 1. On a write miss cycle that is directly followed by a read hit, W/R must be high simultaneously or before /RE goes high.

2. /G becomes a don't care after t_{RGX} during a write miss.

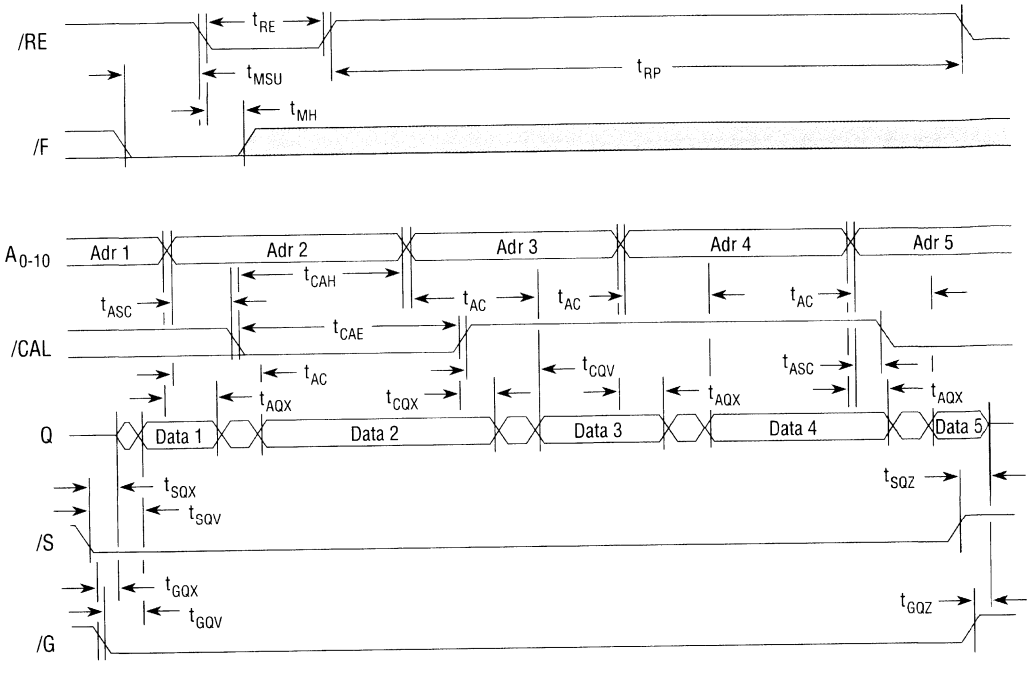
3. t_{CDR} only applies if /CAL falls prior to t_{RAC2} timing interval.

Page Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address 2 modifies only address pin A_9 or A_{10}, then t_{AQX} becomes t_{AQX1}.

/F Refresh (Including "CAS Before RAS") with Page Mode and Static Column Reads

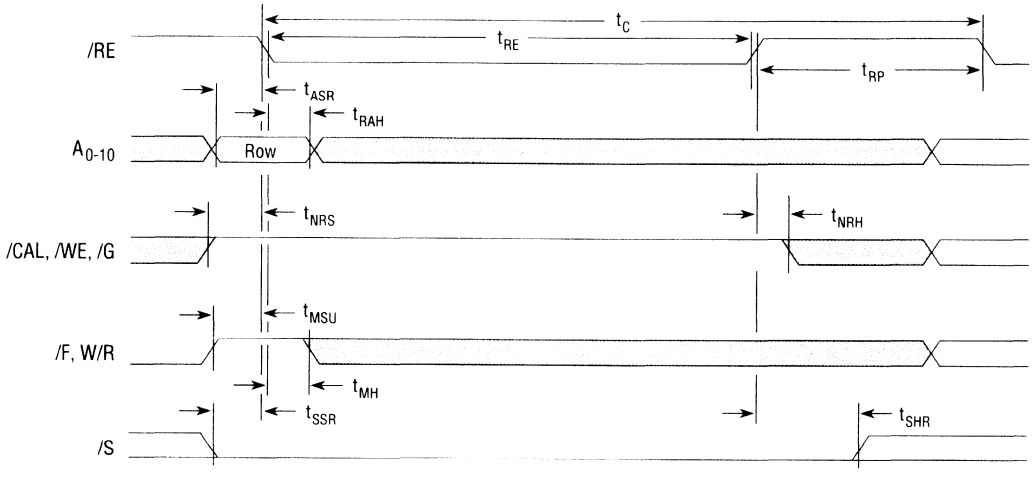


NOTES: 1. During /F refresh cycles, /S is a don't care unless cache reads are performed. For cache reads, /S must be low.

2. If /CAL is low when /RE falls, a "/CAS before /RAS" type refresh occurs.

3. If column address 2, 3, 4, or 5 modifies only address pin A_9 or A_{10}, then t_{AC} becomes t_{AC1} for data 2, 3, 4, and 5, and t_{AQX} becomes t_{AQX1} for data 1, 2, 3, and 4.

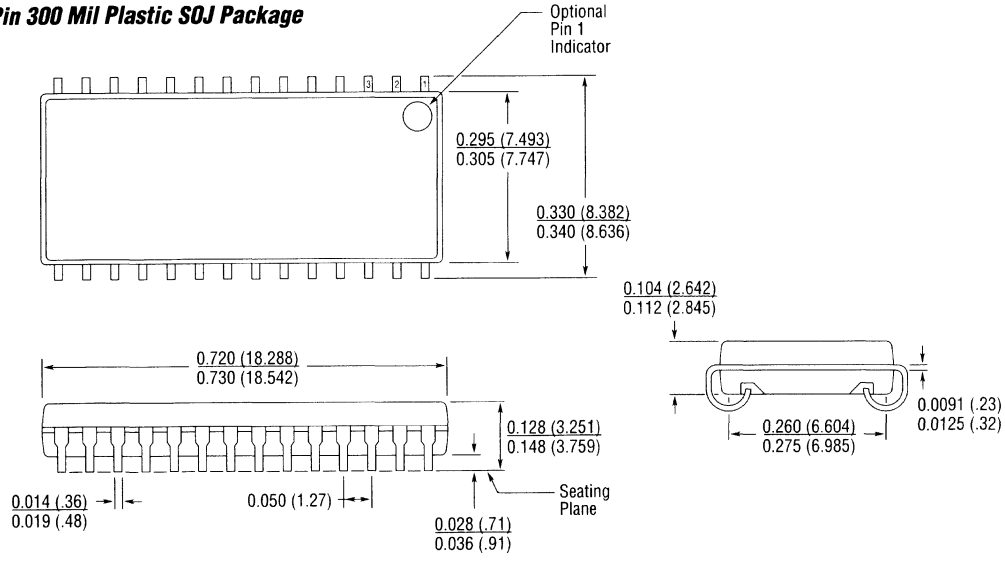
/RE-Only Refresh



NOTES: 1. All binary combinations of $A_{0\text{-}9}$ must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

2

Mechanical Data
28 Pin 300 Mil Plastic SOJ Package



Part Numbering System

DM2200J - 15

Access Time from Cache in Nanoseconds
15ns
20ns

Packaging System
J = 300 Mil, Plastic SOJ

I/O Width
i.e., Power to Which 2 is Raised for I/O Width

Special Features Field
0 = No Write Per Bit
1 = Write Per Bit

Capacity in Bits
i.e., Power to Which 2 is Raised for Total Capacity

Dynamic Memory

DM2202/2212 EDRAM
1Mb x 4 Enhanced Dynamic RAM

Product Specification

Features

- 2Kbit SRAM Cache Memory for 15ns Random Reads Within a Page
- Fast 4Mbit DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- Simple On-chip Page Caching Control Allows DRAM-like System Architecture and Compatibility
- 256-byte Wide DRAM to SRAM Bus for 7.3 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge Cycles
- Hidden Refresh or /CAS Before /RAS Type Refresh Cycles
- Write-per-bit Option (DM2212) for Parity and Video Applications
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- 300 Mil Plastic SOJ Package

Description

The Ramtron 4Mb enhanced DRAM combines raw speed with innovative architecture to offer the optimum cost-performance solution for high performance local or system main memory. In most high speed applications, no-wait-state performance can be achieved without secondary SRAM cache and without interleaving main memory banks at system clock speeds through 40MHz. Two-way interleave will allow no-wait-state operation at clock speeds greater than 66MHz without the need of secondary SRAM cache. The EDRAM outperforms conventional SRAM cache plus DRAM memory systems by minimizing processor wait states for all possible bus events, not just cache hits. The combination of input data and address latching, 2K of fast on-chip SRAM cache, and simplified on-chip cache control allows system level flexibility, performance, and overall memory cost reduction not available with any other high density memory component. Architectural similarity with JEDEC DRAMs allows a single memory controller design to support either slow JEDEC DRAMs or high speed EDRAMs. A system designed in this manner can provide a simple upgrade path to higher system performance.

Architecture

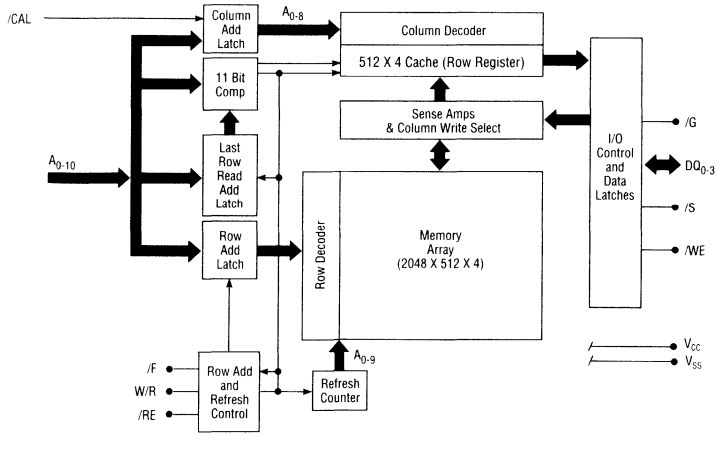
The architecture is similar to a standard 4Mb page mode or static column DRAM with the addition of an integrated cache and internal control which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the internal comparator detects a page hit, only the SRAM is accessed and data is available in 15ns from column address. When a page read miss is detected, the new DRAM row is loaded into the cache and data is available at the output all within 35ns from row enable. Subsequent reads within the page (burst reads or random reads) can continue at 15ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

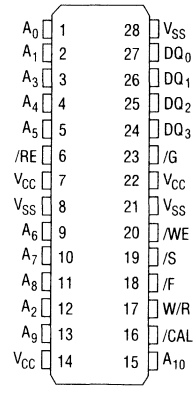
Memory writes are internally posted in 15ns and directed to the DRAM array. During a write hit, the on-chip address comparator

2

Functional Diagram



Pin Configuration



activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 15ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance without any significant increase in die size over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address changes. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	↓	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 15ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time t_{AC} after the column address is setup to /CAL.

Function	/S	/G	/CAL	A_{0-8}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

Write-Per-Bit Operation

The DM2212 version of the 1Mb x 4 EDRAM offers a write-per-bit capability which allows single bits of the memory to be selectively written without altering other bits in the same word. This capability may be useful for implementing parity or masking data in video graphics applications. The bits to be written are determined by a bit mask data word which is placed on the I/O data pins DQ_{0-4} prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F type refresh cycle. When /F type refreshing is used, at least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled. In this case, the output remains disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization.

Unallowed Mode

Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. If these techniques are used, the EDRAM will require only four control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], W/R, and /G). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Pin Descriptions

/RE — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/CAL — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pin during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition; read and write cycles cannot be executed while /S is high. /S must remain active throughout any read or write operation. Only the /F refresh operation can be executed when /S is high.

DQ_{0-3} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2212 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 9-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

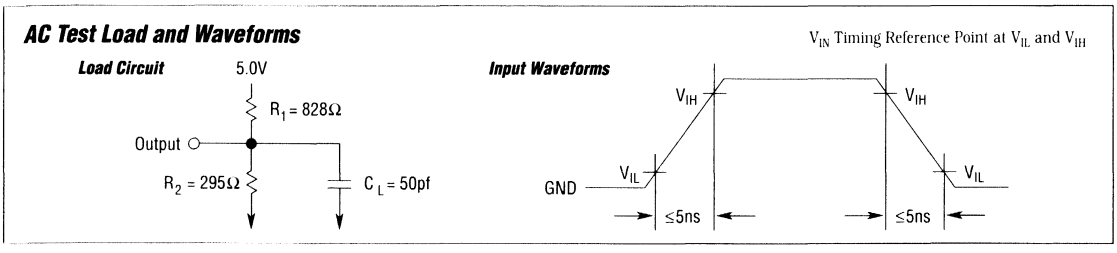
These inputs are connected to the power supply ground connection.

Pin Names

Pin Names	Function
A_{0-10}	Address Inputs
/RE	Row Enable
DQ_{0-3}	Data In/Data Out
/CAL	Column Address Latch
W/R	Write/Read Control
V_{CC}	Power (+5V)

Pin Names	Function
V_{SS}	Ground
/WE	Write Enable
/G	Output Enable
/F	Refresh Control
/S	Chip Select - Active/Standby Control

AC Test Load and Waveforms



Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current (I_{OUT})	50mA*

*One output at a time: short duration.

Capacitance

Description	Max	Pins
Input Capacitance	7pf	A_{0-9}
Input Capacitance	10pf	A_{10}, /CAL, /RE, W/R, /WE, /F, /S
Input Capacitance	2pf	/G
I/O Capacitance	6pf	DQ_{0-3}

Electrical Characteristics

(T_A = 0 - 70°C)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	-10µA	10µA	$0V \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-10µA	10µA	$0V \le V_{IN}$, $0V \le V_{OUT} \le 5.5V$

Symbol	Operating Current	33MHz Typ[1]	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	110mA	225mA	180mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	65mA	145mA	115mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	55mA	110mA	90mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	135mA	190mA	150mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	50mA	135mA	105mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	1mA	1mA	1mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	30mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. In this typical example, page mode and random reads refer to page burst hits and misses. Writes are two clock cycle random and page mode writes. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{AC}[1]	Column Address Access Time		15		20	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		6		ns
t_C	Row Enable Cycle Time	65		85		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
t_{CA}	Address Cycle Time (Cache Hits)	15		20		ns
t_{CAE}	Column Address Latch Active Time	6		7		ns
t_{CDR}[2]	Column Address Delay from /RE Low, After /CAL Assertion in a Write Hit Cycle	35		45		ns
t_{CAH}	Column Address Hold Time	0		1		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		7		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-1		-1		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		17		20	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		6		ns
t_{CWL}	/WE Low to /CAL Inactive	5		7		ns
t_{DH}	Data Input Hold Time	0		1		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1.5		2		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		6		ns
t_{DS}	Data Input Setup Time	5		6		ns
t_{GQV}[1]	Output Enable Access Time		5		6	ns
t_{GQX}[3,4]	Output Enable to Output Drive Time	0	5	0	6	ns
t_{GQZ}[5,6]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	6	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		1		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		6		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
t_{PC}	Column Address Latch Cycle Time	15		20		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		35		45	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		17		22	ns
t_{RAC2}[1,7]	Row Enable Access Time for a Cache Write Hit		35		45	ns
t_{RAH}	Row Address Hold Time	1.5		2		ns
t_{RE}	Row Enable Active Time	35	100000	45	100000	ns

Switching Characteristics (continued)

(V_{CC} = 5V ± 5%, T_A = 0 - 70°C), C_L = 50pf

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	10		13		ns
t_{RP}(8)	Row Precharge Time	25		32		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		1		ns
t_{RSH}	Last Write Address Latch to End of Write	15		20		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	40		51		ns
t_{RWL}	Last Write Enable to End of Write	15		20		ns
t_{SC}	Column Address Cycle Time	15		20		ns
t_{SHR}	Select Hold From Row Enable	0		1		ns
t_{SQV}(1)	Chip Select Access Time		15		20	ns
t_{SQX}(3,4)	Output Turn-On From Select Low	0	15	0	20	ns
t_{SQZ}(5,6)	Output Turn-Off From Chip Select	0	10	0	13	ns
t_{SSR}	Select Setup Time to Row Enable	5		6		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	15		20		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
t_{WHR}(9)	Write Enable Hold After /RE	0		1		ns
t_{WI}	Write Enable Inactive Time	5		7		ns
t_{WP}	Write Enable Active Time	5		7		ns
t_{WQV}(1)	Data Valid From Write Enable High		15		20	ns
t_{WQX}(3,6)	Data Output Turn-On From Write Enable High	0	15	0	20	ns
t_{WQZ}(4,5)	Data Turn-Off From Write Enable Low	0	15	0	20	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Cache Miss)		15		20	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Column Address is Ignored Prior to t_{CDR} for This Specific Cycle

(3) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(4) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

(5) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

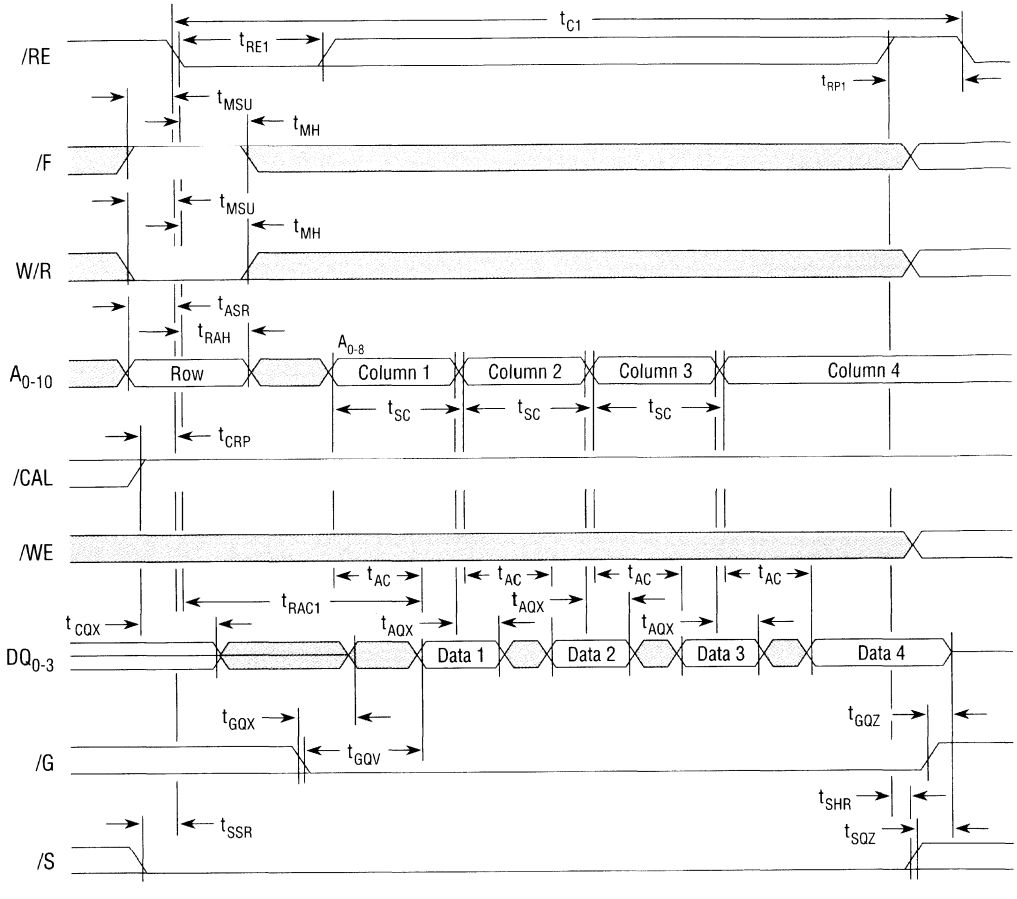
(6) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(7) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

(8) For Back-to-Back /F Refreshes, t_{RP} = 40ns. For Non-consecutive /F Refreshes, t_{RP} = 25ns and 32ns Respectively

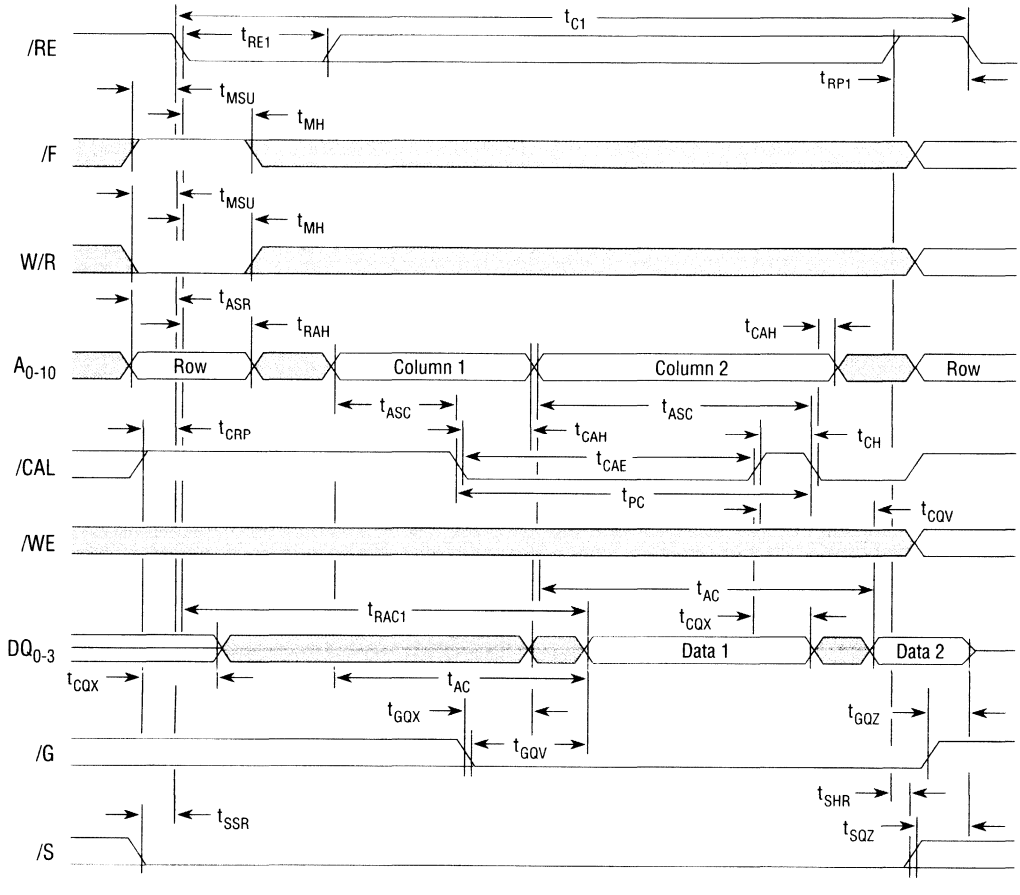
(9) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

/RE Active Cache Read Hit (Static Column Mode)

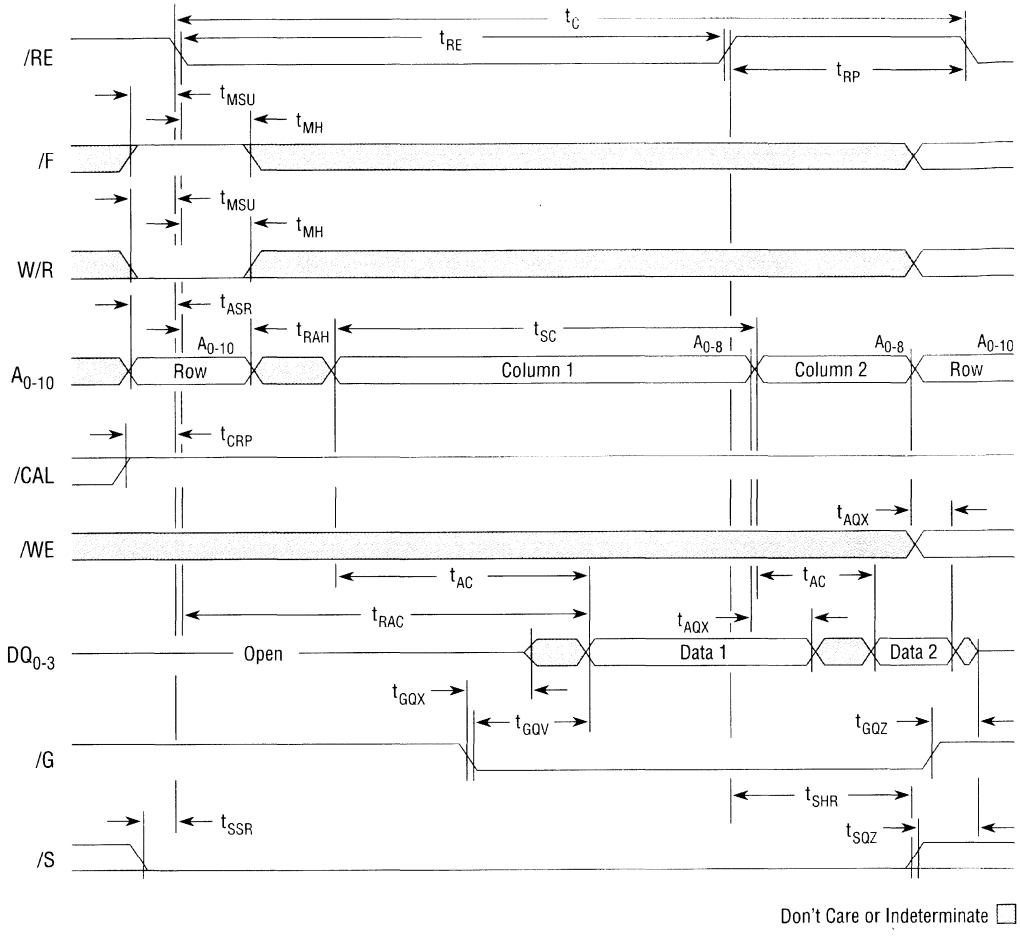


Don't Care or Indeterminate ☐

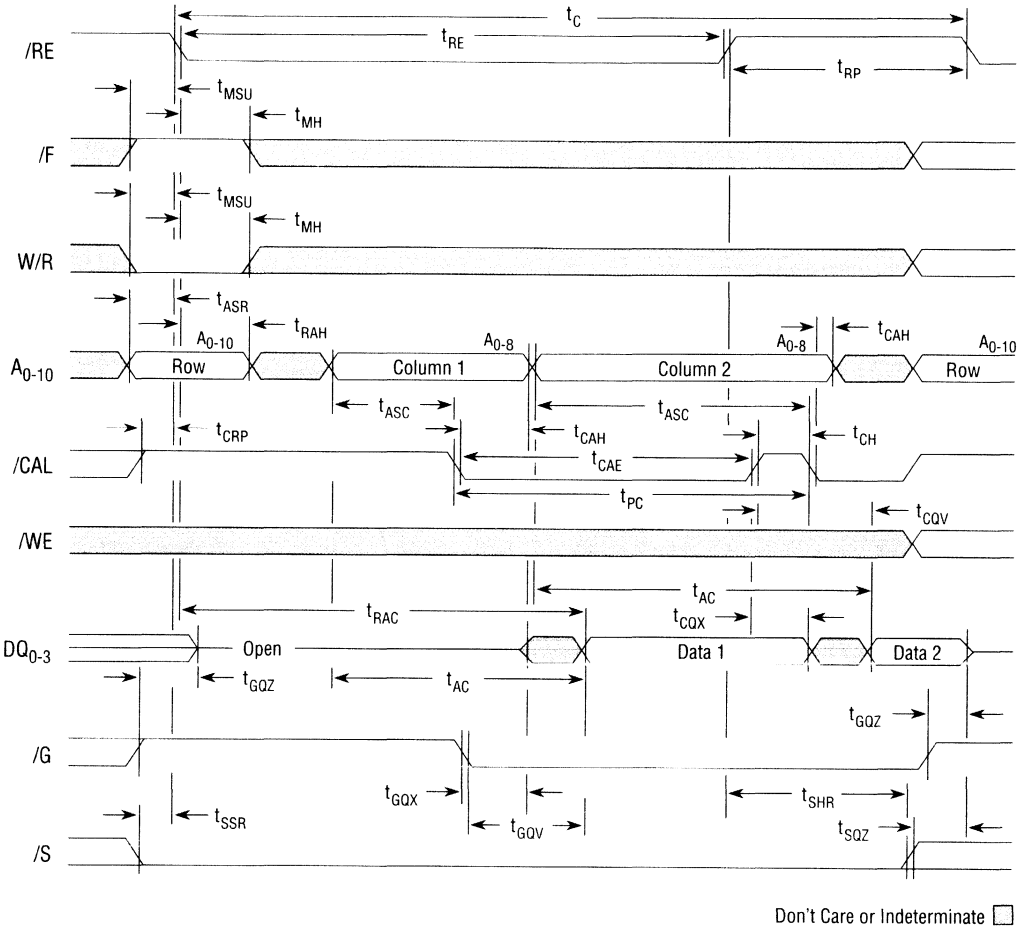
/RE Active Cache Read Hit (Page Mode)



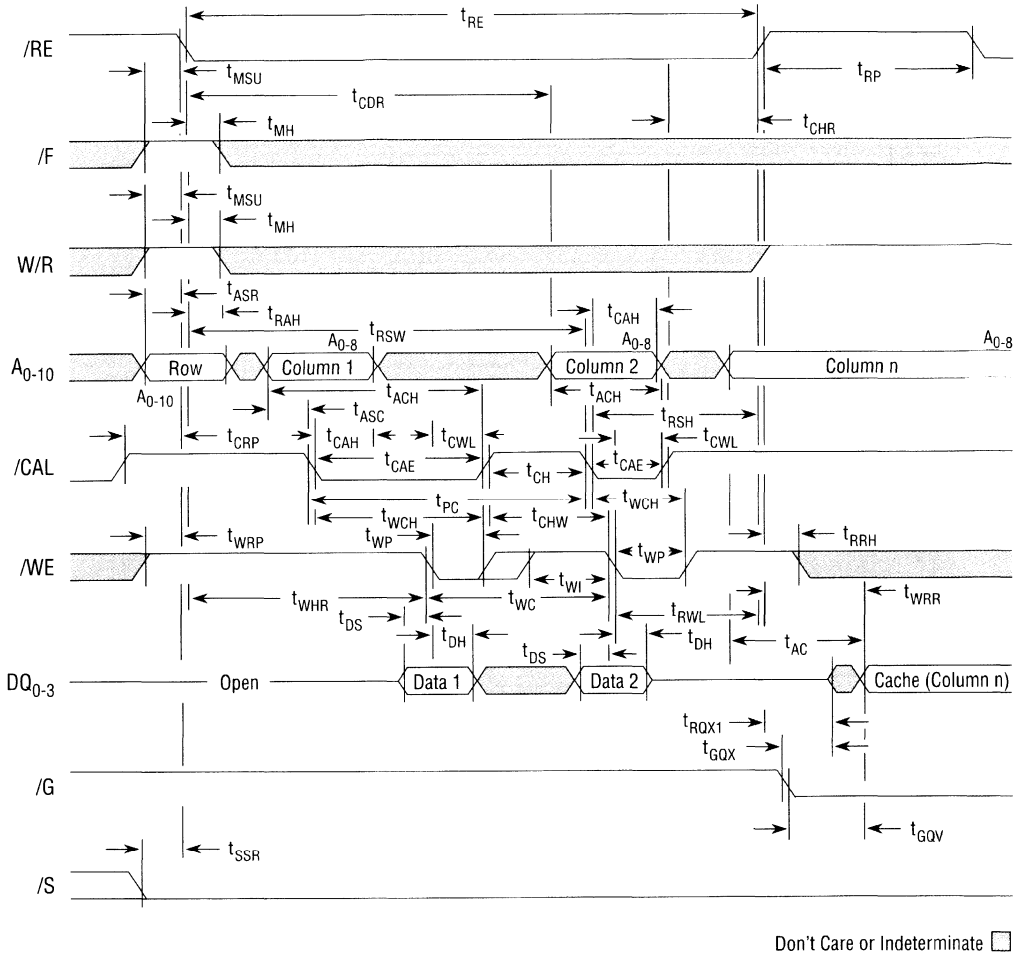
/RE Active Cache Read Miss (Static Column Mode)



/RE Active Cache Read Miss (Page Mode)



Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads

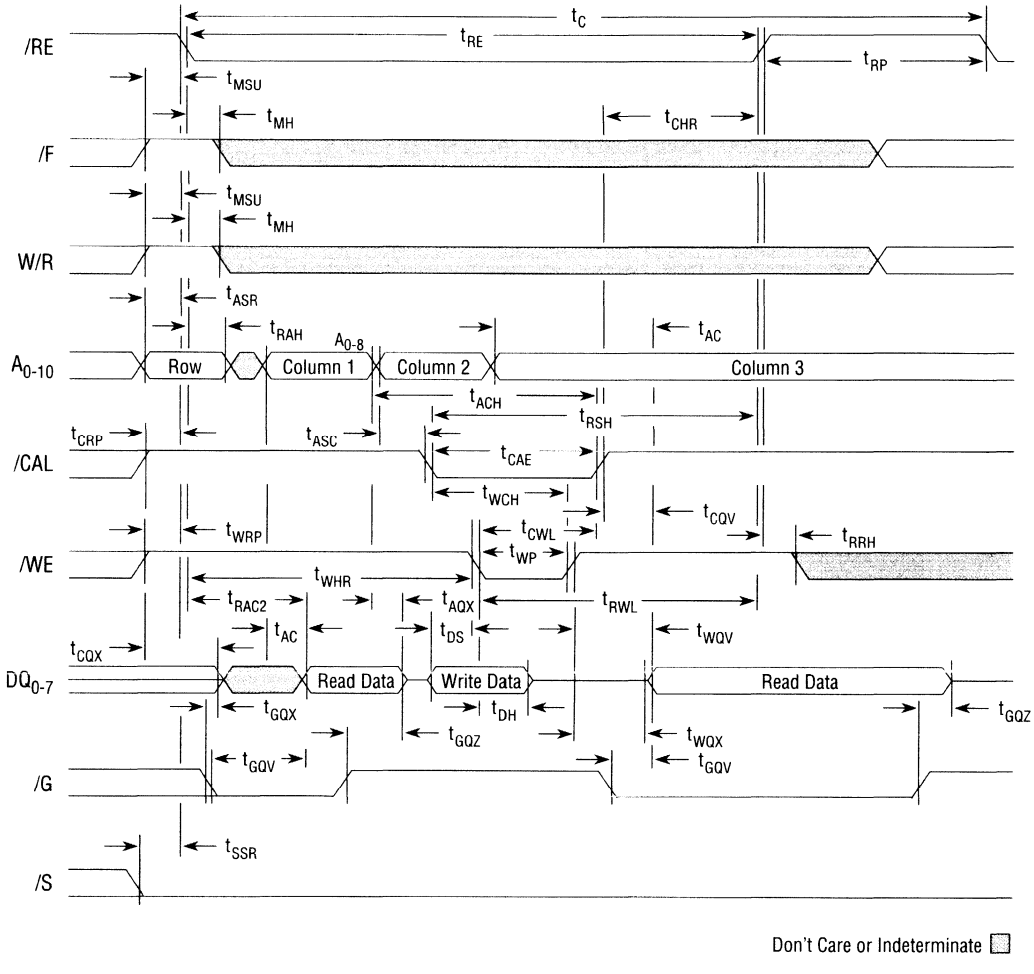


NOTES: 1. On a write miss cycle that is directly followed by a read hit, W/R must be high simultaneously or before /RE goes high.

2. /G becomes a don't care after t_{RGX} during a write miss.

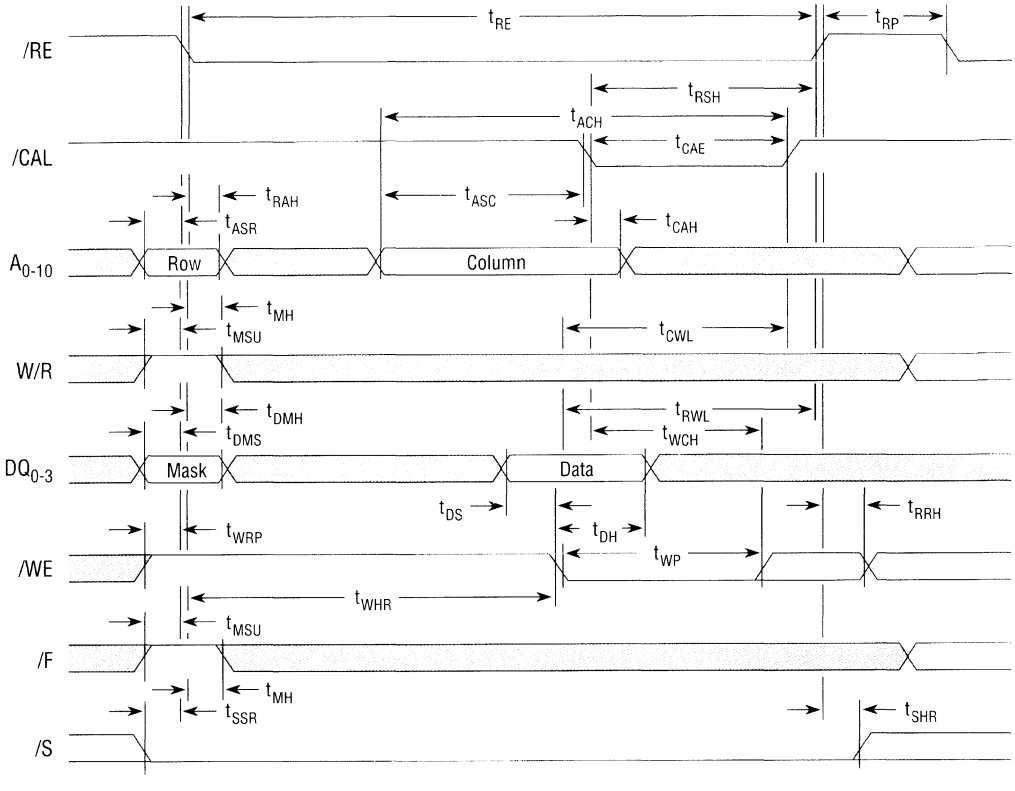
3. t_{CDR} only applies if /CAL falls prior to t_{RAC2} timing interval.

Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address one equals column address two, then a read-modify-write cycle is performed.

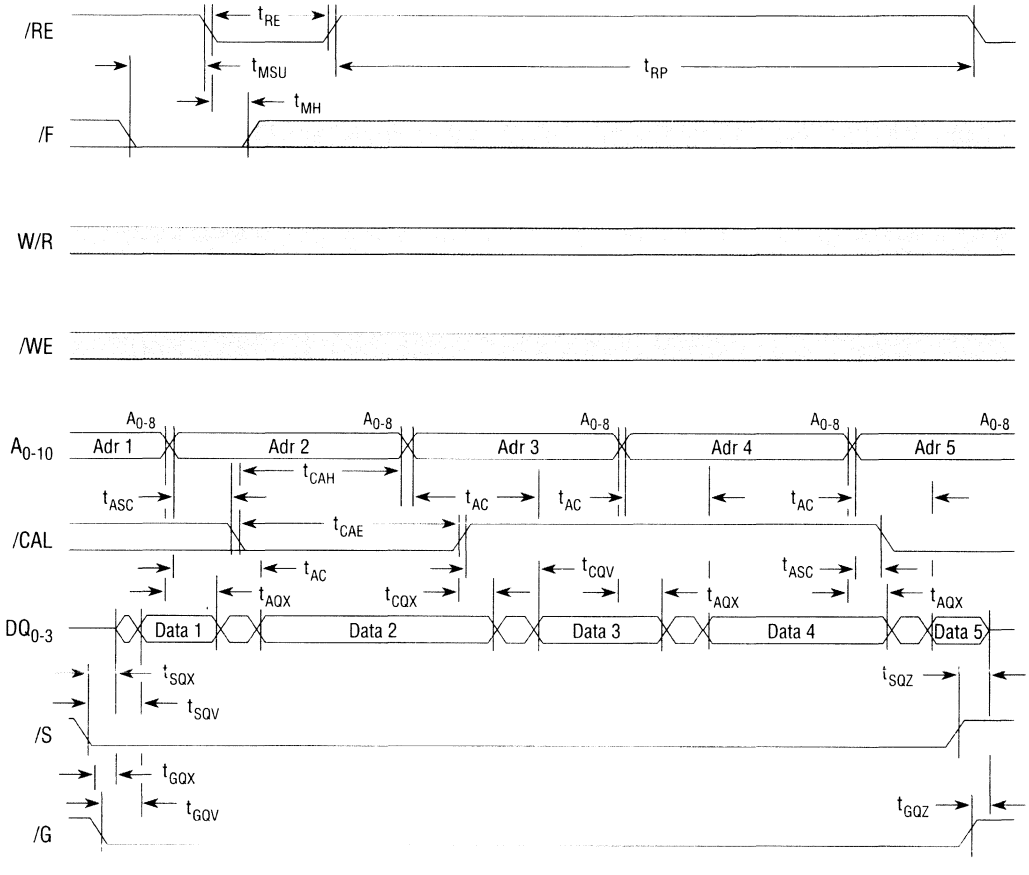
Write-Per-Bit Cycle (/G=High)



NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.

2. Two X4 EDRAM options are available, one with write-per-bit (DM2212) and one without write-per-bit (DM2202).

/F Refresh (Including "CAS Before RAS") With Page Mode and Static Column Cache Reads

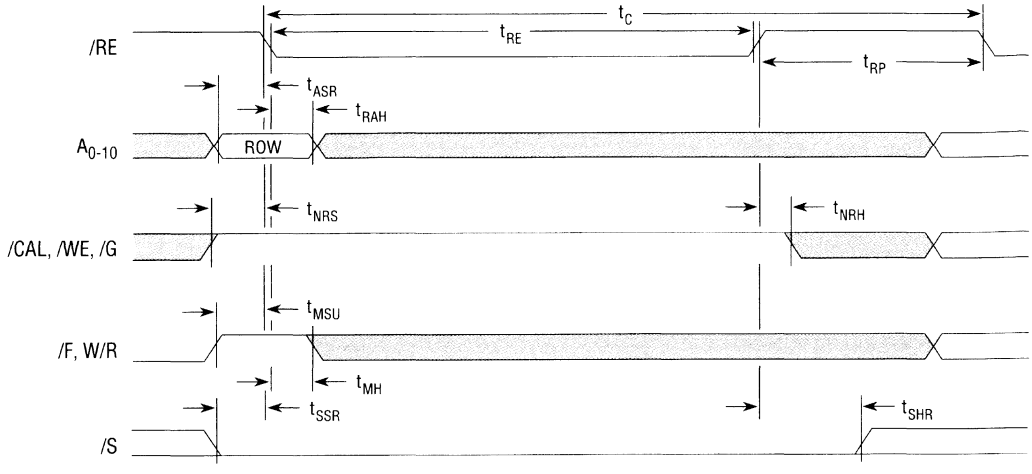


Don't Care or Indeterminate ☐

NOTES: 1. During /F refresh cycles, /S is a don't care unless cache reads are performed. For cache reads, /S must be low.

2. If /CAL is low when /RE falls, a "CAS before RAS" type refresh occurs.

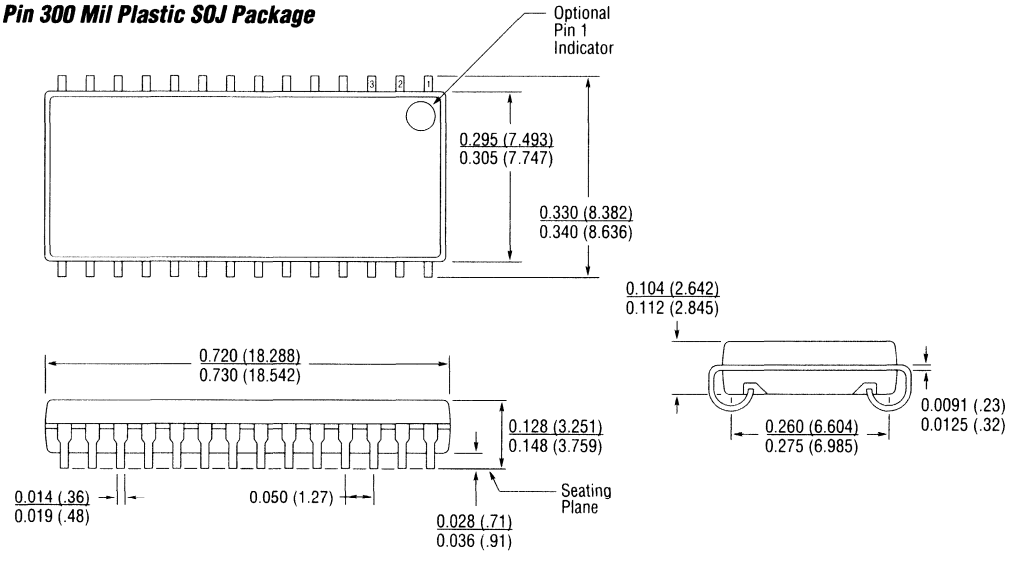
/RE-Only Refresh



Don't Care or Indeterminate ☐

NOTES: 1. All binary combinations of A_{0-9} must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

Mechanical Data
28 Pin 300 Mil Plastic SOJ Package



Part Numbering System

2

DM2202J - 15

Access Time from Cache in Nanoseconds
15ns
20ns

Packaging System
J = 300 Mil, Plastic SOJ

I/O Width
i.e., Power to Which 2 is Raised for I/O Width

Special Features Field
0 = No Write Per Bit
1 = Write Per Bit

Capacity in Bits
i.e., Power to Which 2 is Raised for Total Capacity

Dynamic Memory

DM1M36SJ/DM1M32SJ
1Mbx36/1Mbx32 Enhanced DRAM SIMM

Product Specification

Features

- 2Kbyte SRAM Cache Memory for 15ns Random Reads Within a Page
- Fast DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- Simple On-chip Page Caching Control Allows DRAM-like System Architecture and Compatibility
- 2Kbyte Wide DRAM to SRAM Bus for 58.6 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge Cycles
- Hidden Refresh or /CAS Before /RAS Type Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- Compatibility with JEDEC 1M x 36 DRAM SIMM Configuration Allows Performance Upgrade in System

Description

The Ramtron 4Mb enhanced DRAM SIMM module provides a single memory module solution for the main memory or local memory of fast PCs, workstations, servers, and other high performance systems. Due to its fast 15ns cache row register, the EDRAM memory module supports zero-wait-state burst read operations at up to 40MHz bus rates in a non-interleave configuration and >66MHz bus rates with a two-way interleave configuration.

On-chip write posting and fast page mode operation supports 15ns write and burst write operations. On a cache miss, the fast DRAM array reloads the entire 2Kbyte cache over a 2Kbyte-wide bus in 35ns for an effective bandwidth of 58 Gbytes/sec. This means very low latency and fewer wait states on a cache miss than a non-integrated cache/DRAM solution. The JEDEC compatible 72-bit SIMM configuration allows a single memory controller to be designed to support either JEDEC slow DRAMs or high speed EDRAMs to provide a simple upgrade path to higher system performance.

Architecture

The DM1M36SJ achieves 1Mb x 36 density by mounting nine 1M x 4 EDRAMs, packaged in 28-pin plastic SOJ packages, on a multi-layer substrate. Eight DM2202 devices and one DM2212 device provide data and parity storage. The DM1M32SJ contains eight DM2202 devices for data only.

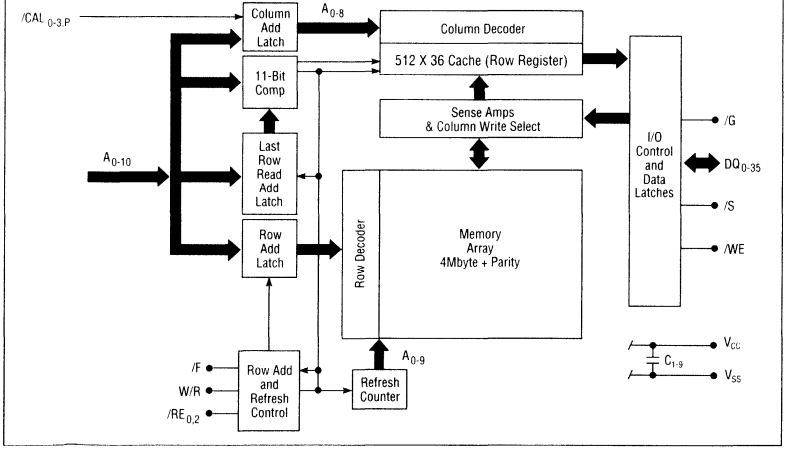
The EDRAM memory module architecture is very similar to a standard 4MB DRAM module with the addition of an integrated cache and on-chip control which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the on-chip comparator detects a page hit, only the SRAM is accessed and data is available in 15ns from column address. When a page read miss is detected, the entire new DRAM row is loaded into the cache and data is available at the output all within 35ns from row enable. Subsequent reads within the page (burst reads or random reads) will continue at 15ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

Memory writes are internally posted in 15ns and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 15ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the

Functional Diagram



2

 1850 Ramtron Drive, Colorado Springs, CO 80921
Telephone (719) 481-7000, Fax (719) 488-9095

EDRAM is able to provide superior performance without any significant increase in die size over standard slow 4Mb DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address changes. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 15ns cycle times (the first read cannot complete until after

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	↓	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time t_{AC} after the column address is setup to /CAL.

Function	/S	/G	/CAL	A_{0-8}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

Write-Per-Bit Operation

The DM1M36SJ EDRAM SIMM provides a write-per-bit capability to selectively modify individual parity bits ($DQ_{8,17,26,35}$) for byte write operations. The parity device (DM2212) is selected via $/CAL_P$. Data bits do not require or support write-per-bit capability. Byte write selection to non-parity bits is accomplished via $/CAL_{0-3}$. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F type refresh cycle. When /F type refreshing is used, at least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled. In this case, the output remains disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization.

Unallowed Mode

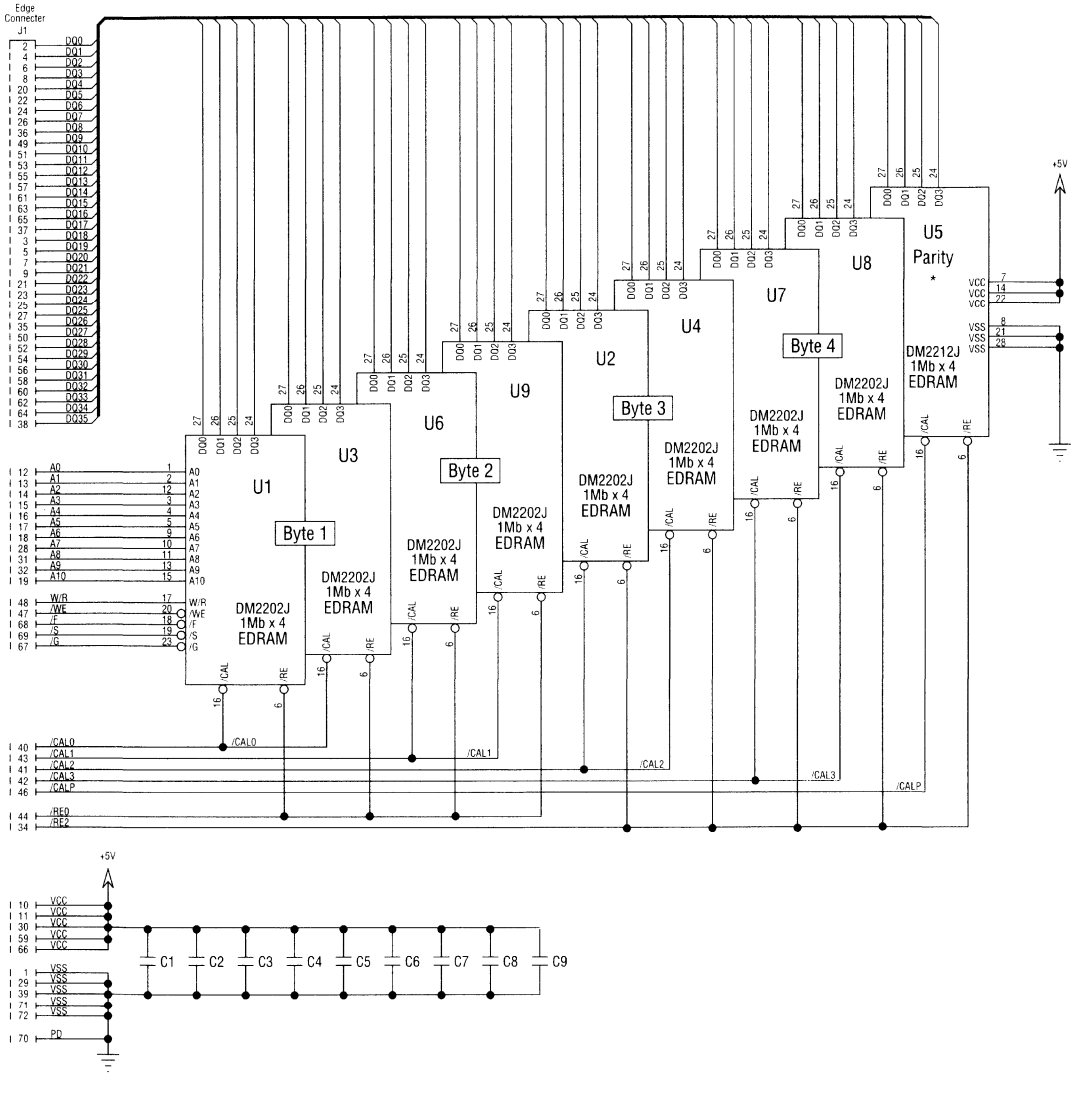
Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or

more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. If these techniques are used, the EDRAM will require only four control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], W/R, and /G). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

Interconnect Diagram



*DM2212 (U5) is not present on the DM1M32SJ.

Pinout

Pin No.	Function	Interconnect (Component Pin)	Organization
1	GND	C (8, 21, 28)	Ground
2	DQ_0	U1 (27)	Byte 1 I/O 1
3	DQ_{18}	U2 (24)	Byte 3 I/O 1
4	DQ_1	U1 (26)	Byte 1 I/O 2
5	DQ_{19}	U2 (25)	Byte 3 I/O 2
6	DQ_2	U1 (25)	Byte 1 I/O 3
7	DQ_{20}	U2 (26)	Byte 3 I/O 3
8	DQ_3	U1 (24)	Byte 1 I/O 4
9	DQ_{21}	U2 (27)	Byte 3 I/O 4
10	+5 Volts	C (7, 14, 22)	V_{CC}
11	+5 Volts	C (7, 14, 22)	V_{CC}
12	A_0	C (1)	Address
13	A_1	C (2)	Address
14	A_2	C (12)	Address
15	A_3	C (3)	Address
16	A_4	C (4)	Address
17	A_5	C (5)	Address
18	A_6	C (9)	Address
19	A_{10}	C (15)	Address
20	DQ_4	U3 (27)	Byte 1 I/O 5
21	DQ_{22}	U4 (24)	Byte 3 I/O 5
22	DQ_5	U3 (26)	Byte 1 I/O 6
23	DQ_{23}	U4 (25)	Byte 3 I/O 6
24	DQ_6	U3 (25)	Byte 1 I/O 7
25	DQ_{24}	U4 (26)	Byte 3 I/O 7
26	DQ_7	U3 (24)	Byte 1 I/O 8
27	DQ_{25}	U4 (27)	Byte 3 I/O 8
28	A_7	C (10)	Address
29	GND	C (8, 21, 28)	Ground
30	+5 Volts	C (7, 14, 22)	V_{CC}
31	A_8	C (11)	Address
32	A_9	C (13)	Address
33	NC		Reserved for 2Mb x 36
34	$/RE_2$	U2,4,5,7,8 (6)	Row Enable (Bytes 3,4, Parity)
35	DQ_{26}*	U5 (27)	Parity I/O for Byte 3
36	DQ_8*	U5 (26)	Parity I/O for Byte 1
37	DQ_{17}*	U5 (25)	Parity I/O for Byte 2
38	DQ_{35}*	U5 (24)	Parity I/O for Byte 4
39	GND	C (8, 21, 28)	Ground
40	$/CAL_0$	U1,3 (16)	Byte 1 Column Address Latch
41	$/CAL_2$	U2,4 (16)	Byte 3 Column Address Latch
42	$/CAL_3$	U7,8 (16)	Byte 4 Column Address Latch
43	$/CAL_1$	U6,9 (16)	Byte 2 Column Address Latch
44	$/RE_0$	U1,3,6,9 (6)	Row Enable (Bytes 1,2)
45	NC		Reserved for 2Mb x 36
46	$/CAL_P$*	U5 (16)	Parity Column Address Latch
47	/WE	C (20)	Write Enable
48	W/R	C (17)	W/R Mode Control
49	DQ_9	U6 (27)	Byte 2 I/O 1
50	DQ_{27}	U7 (27)	Byte 4 I/O 1
51	DQ_{10}	U6 (26)	Byte 2 I/O 2
52	DQ_{28}	U7 (26)	Byte 4 I/O 2
53	DQ_{11}	U6 (25)	Byte 2 I/O 3
54	DQ_{29}	U7 (25)	Byte 4 I/O 3
55	DQ_{12}	U6 (24)	Byte 2 I/O 4
56	DQ_{30}	U7 (24)	Byte 4 I/O 4
57	DQ_{13}	U9 (24)	Byte 2 I/O 5
58	DQ_{31}	U8 (27)	Byte 4 I/O 5
59	+5 Volts	C (7, 14, 22)	V_{CC}
60	DQ_{32}	U8 (26)	Byte 4 I/O 6
61	DQ_{14}	U9 (25)	Byte 2 I/O 6
62	DQ_{33}	U8 (25)	Byte 4 I/O 7
63	DQ_{15}	U9 (26)	Byte 2 I/O 7
64	DQ_{34}	U8 (24)	Byte 4 I/O 8
65	DQ_{16}	U9 (27)	Byte 2 I/O 8
66	+5 Volts	C (7, 14, 22)	V_{CC}
67	/G	C (23)	Output Enable
68	/F	C (18)	Refresh Mode Control
69	/S	C (19)	Chip Select
70	PD	Signal GND	Presence Detect
71	GND	C (8, 21, 28)	Ground
72	GND	C (8, 21, 28)	Ground

C = Common to All Memory Chips, U1 = Chip 1, etc.

*No Connect for DM1M32SJ

Pin Descriptions

/$RE_{0,2}$ — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/$CAL_{0-3,P}$ — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pin during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition; read and write cycles cannot be executed while /S is high. /S must remain active throughout any read or write operation. Only the /F refresh operation can be executed when /S is high.

DQ_{0-35} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2212 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 9-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current (I_{OUT})	50mA*

* One output at a time per device; short duration

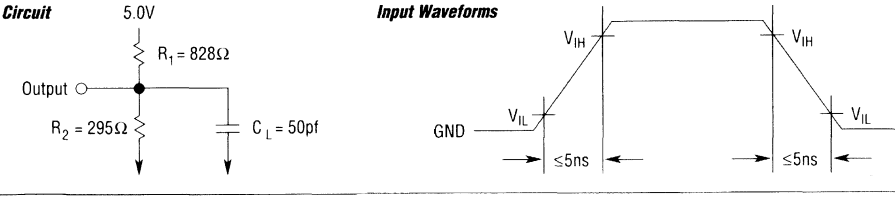
Capacitance

Description	Max*	Pins
Input Capacitance	66/73pf	A_{0-9}
Input Capacitance	90/100pf	A_{10}, W/R, /WE, /F, /S
Input Capacitance	45pf	/RE_0
Input Capacitance	46/56pf	/RE_2
Input Capacitance	26/28pf	/G
Input Capacitance	24pf	/CAL_{0-3}
Input Capacitance	12pf	/CAL_P
I/O Capacitance	8pf	DQ_{0-35}

* DM1M32SJ/DM1M36SJ. respectively

AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}



Electrical Characteristics

(T_A = 0 - 70°C)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	-10µA	10µA	$OV \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-10µA	10µA	$OV \le V_{IN}$, $OV \le V_{OUT} \le 5.5V$

Operating Current — DM1M32SJ

Symbol	Operating Current	33MHz Typ[1]	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	880mA	1800mA	1440mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	520mA	1160mA	920mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	440mA	880mA	720mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	1080mA	1520mA	1200mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	400mA	1080mA	840mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	8mA	8mA	8mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	240mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

Operating Current — DM1M36SJ

Symbol	Operating Current	33MHz Typ[1]	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	990mA	2025mA	1620mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	585mA	1305mA	1035mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	495mA	990mA	810mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	1215mA	1710mA	1350mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	450mA	1215mA	945mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	9mA	9mA	9mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	270mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. In this typical example, page mode and random reads refer to page burst hits and misses. Writes are two clock cycle random and page mode writes. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

Discrete devices have been tested from 4.7V to 5.3V V_{CC} and to 75°C to guarantee SIMM specifications. (V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50pf)

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{AC}[1]	Column Address Access Time		15		20	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
t_{AOX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		6		ns
t_C	Row Enable Cycle Time	65		85		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
t_{CA}	Address Cycle Time (Cache Hits)	15		20		ns
t_{CAE}	Column Address Latch Active Time	6		7		ns
t_{CAH}	Column Address Hold Time	0		1		ns
t_{CDR}[2]	Column Address Delay from /RE Low, After /CAL Assertion in a Write Hit Cycle	35		45		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		7		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-1		-1		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		17		20	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		6		ns
t_{CWL}	/WE Low to /CAL Inactive	5		7		ns
t_{DH}	Data Input Hold Time	0		1		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1.5		2		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		6		ns
t_{DS}	Data Input Setup Time	5		6		ns
t_{GQV}[1]	Output Enable Access Time		5		6	ns
t_{GQX}[3,4]	Output Enable to Output Drive Time	0	5	0	6	ns
t_{GQZ}[5,6]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	6	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		1		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		6		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
t_{PC}	Column Address Latch Cycle Time	15		20		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		35		45	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		17		22	ns
t_{RAC2}[1,7]	Row Enable Access Time for a Cache Write Hit		35		45	ns
t_{RAH}	Row Address Hold Time	1.5		2		ns
t_{RE}	Row Enable Active Time	35	100000	45	100000	ns

Switching Characteristics (continued)

Discrete devices have been tested from 4.7V to 5.3V V_{CC} and to 75°C to guarantee SIMM specifications. (V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50pf)

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	10		13		ns
t_{RP}(8)	Row Precharge Time	25		32		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		1		ns
t_{RSH}	Last Write Address Latch to End of Write	15		20		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	40		51		ns
t_{RWL}	Last Write Enable to End of Write	15		20		ns
t_{SC}	Column Address Cycle Time	15		20		ns
t_{SHR}	Select Hold From Row Enable	0		1		ns
t_{SQV}(1)	Chip Select Access Time		15		20	ns
t_{SQX}(3,4)	Output Turn-On From Select Low	0	15	0	20	ns
t_{SQZ}(5.6)	Output Turn-Off From Chip Select	0	10	0	13	ns
t_{SSR}	Select Setup Time to Row Enable	5		6		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	15		20		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
t_{WHR}(9)	Write Enable Hold After /RE	0		1		ns
t_{WI}	Write Enable Inactive Time	5		7		ns
t_{WP}	Write Enable Active Time	5		7		ns
t_{WQV}(1)	Data Valid From Write Enable High		15		20	ns
t_{WQX}(3.6)	Data Output Turn-On From Write Enable High	0	15	0	20	ns
t_{WQZ}(4.5)	Data Turn-Off From Write Enable Low	0	15	0	20	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Cache Miss)		15		20	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Column Address is Ignored Prior to t_{CDR} for This Specific Cycle

(3) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(4) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

(5) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

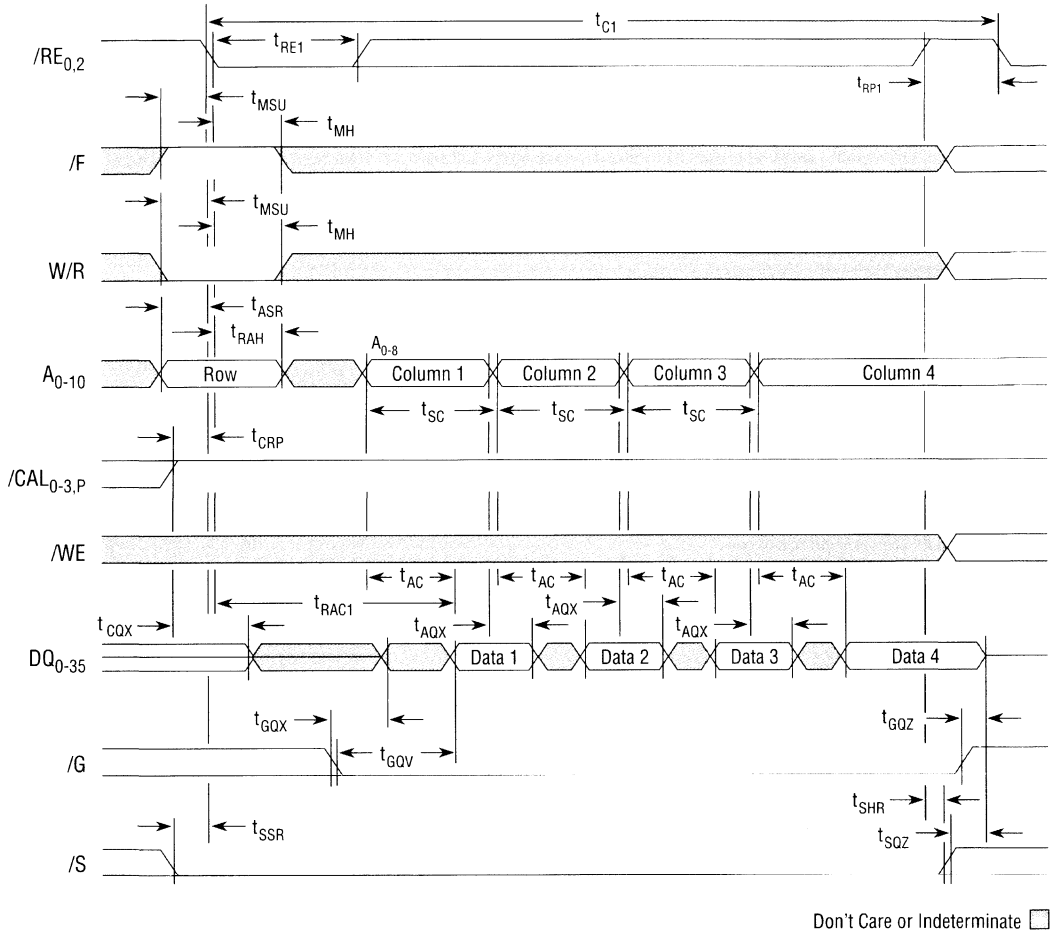
(6) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(7) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

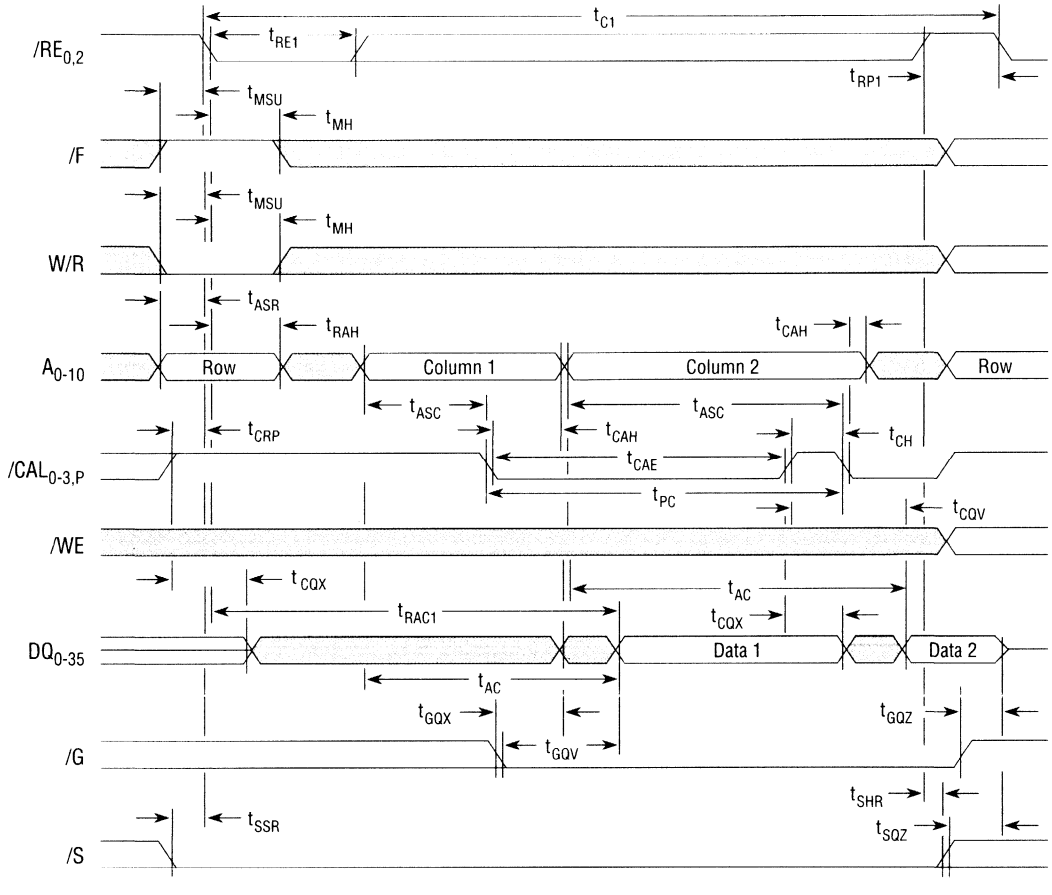
(8) For Back-to-Back /F Refreshes, t_{RP} = 40ns. For Non-consecutive /F Refreshes, t_{RP} = 25ns and 32ns Respectively

(9) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

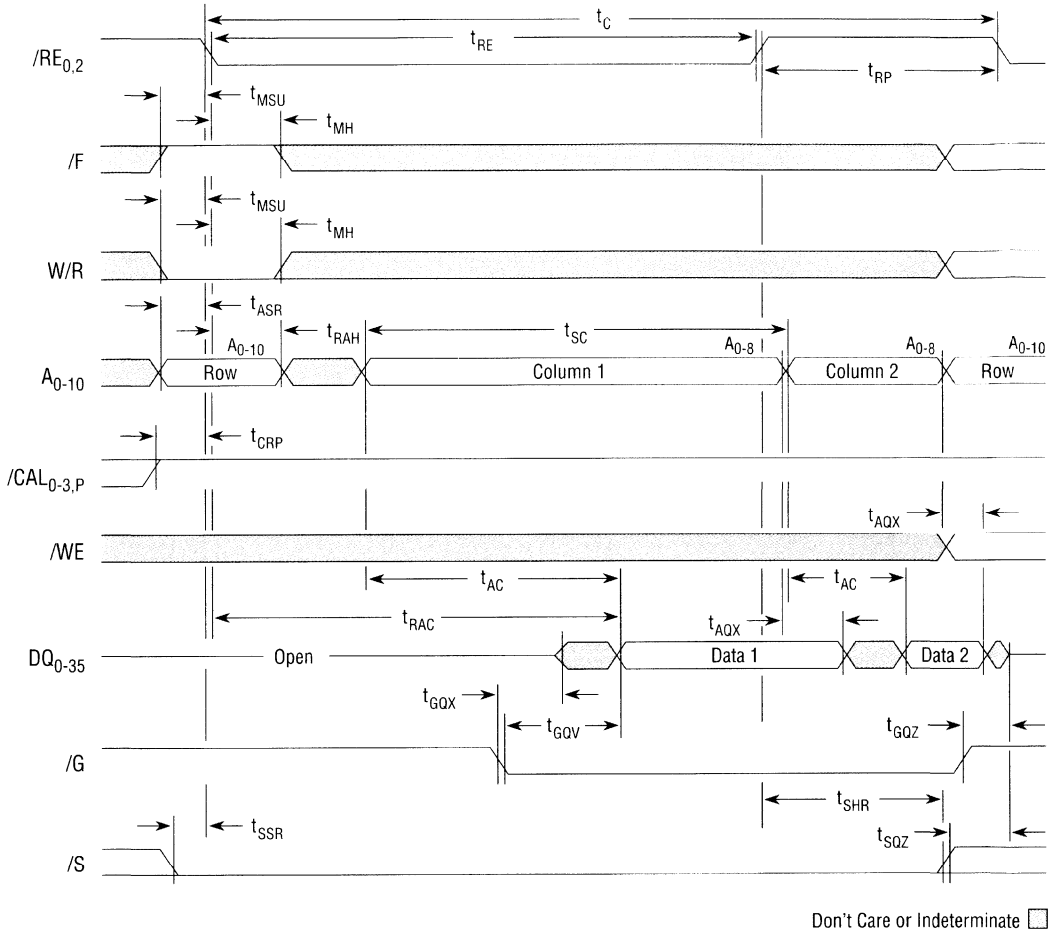
/RE Active Cache Read Hit (Static Column Mode)



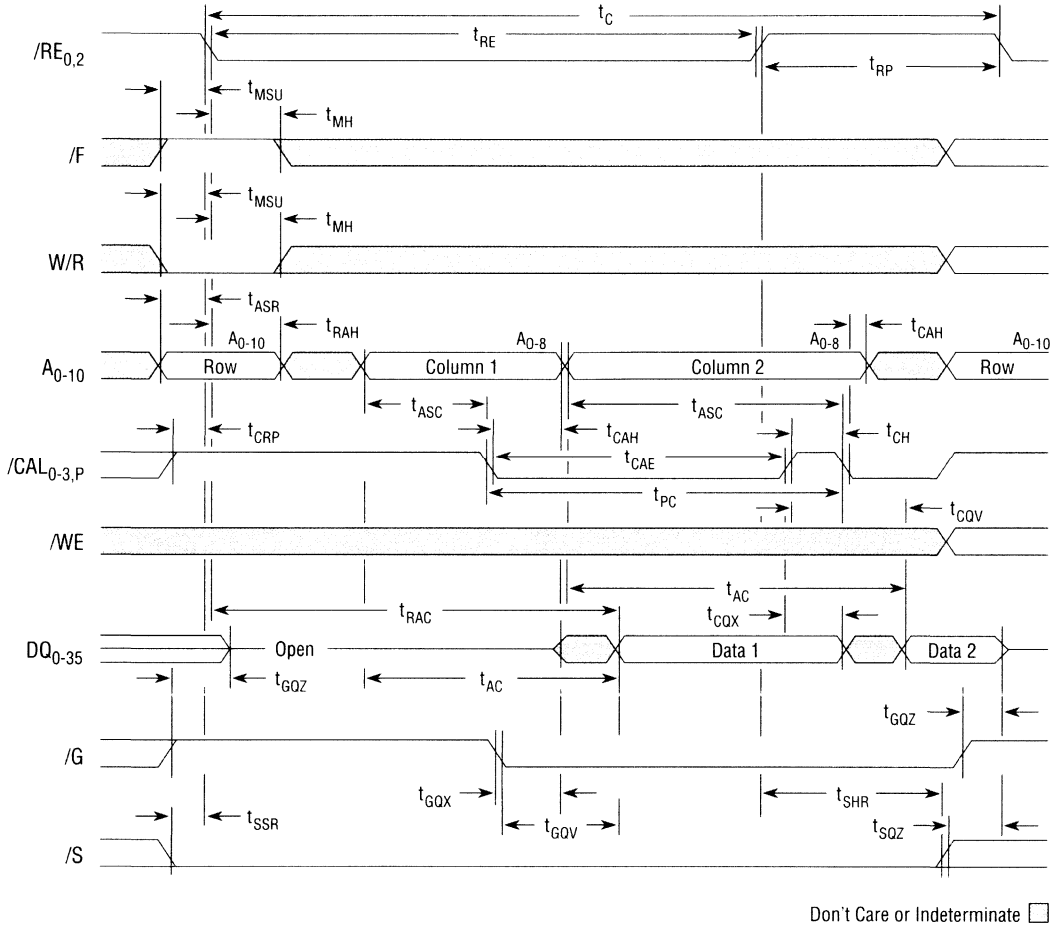
/RE Active Cache Read Hit (Page Mode)



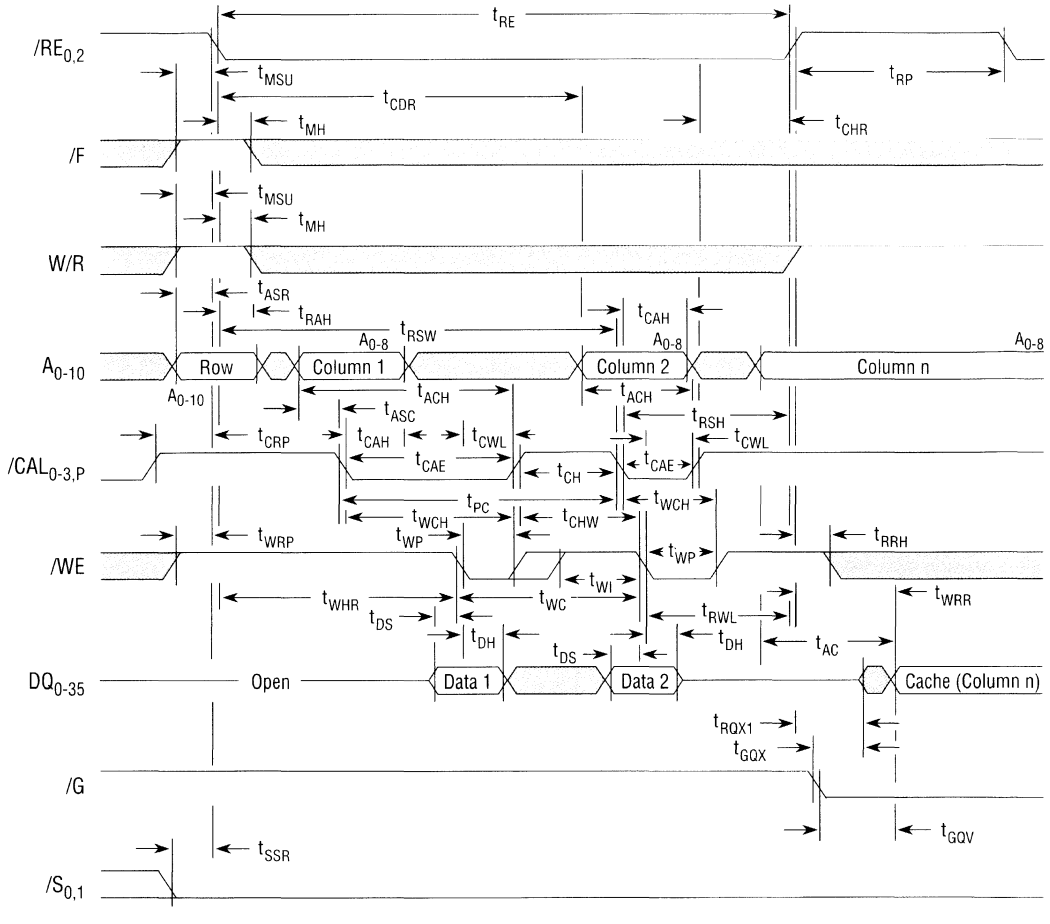
/RE Active Cache Read Miss (Static Column Mode)



/RE Active Cache Read Miss (Page Mode)



Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



Don't Care or Indeterminate ☐

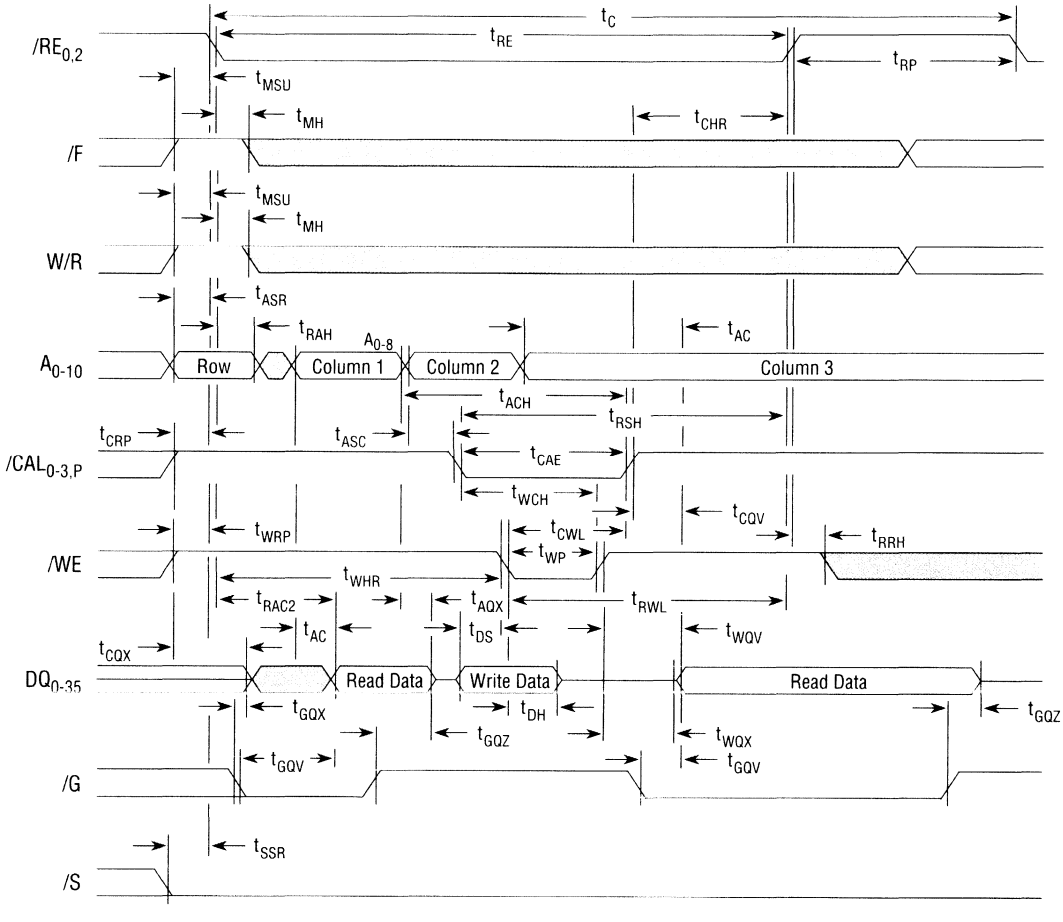
NOTES: 1. Parity bits $DQ_{8,17,26,35}$ must have mask provided at falling edge of /RE.

2. On a write miss cycle that is directly followed by a read hit, W/R must be high simultaneously or before /RE goes high.

3. /G becomes a don't care after t_{RGX} during a write miss.

4. t_{CDR} only applies if /CAL falls prior to t_{RAC2} timing interval.

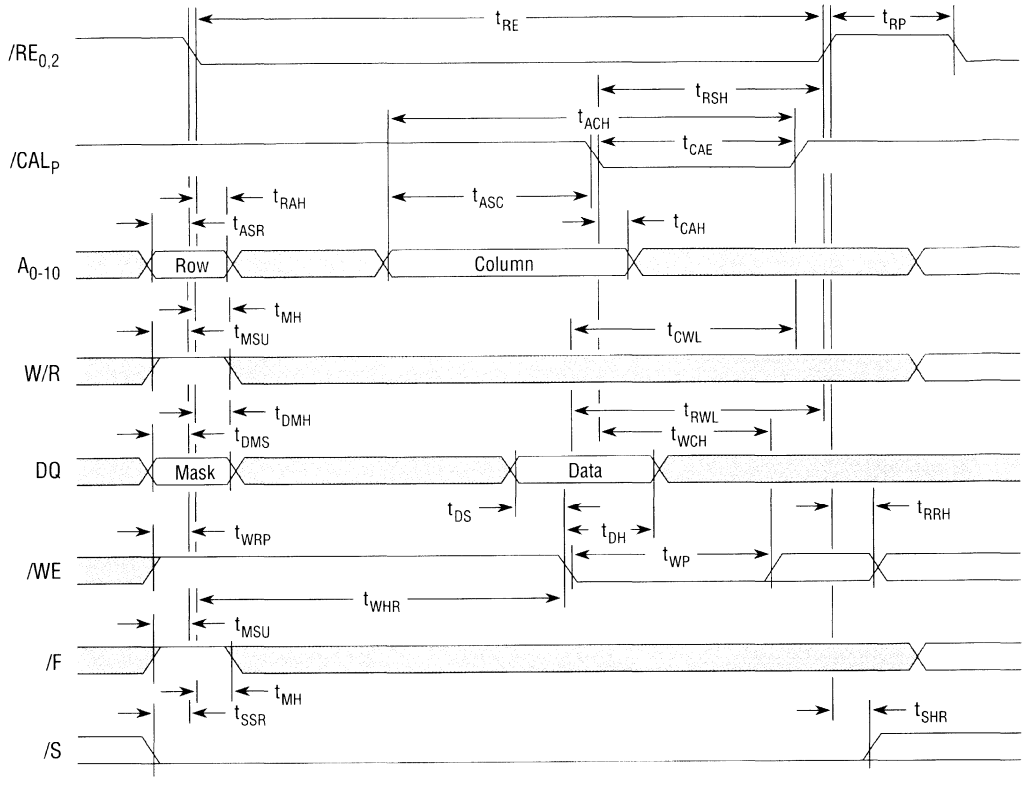
Page Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address 1 equals column address 2, then a read-modify-write cycle is performed.

2. Parity bits $DQ_{8,17,26,35}$ must have mask provided at falling edge of /RE.

Write-Per-Bit Cycle (/G = High)

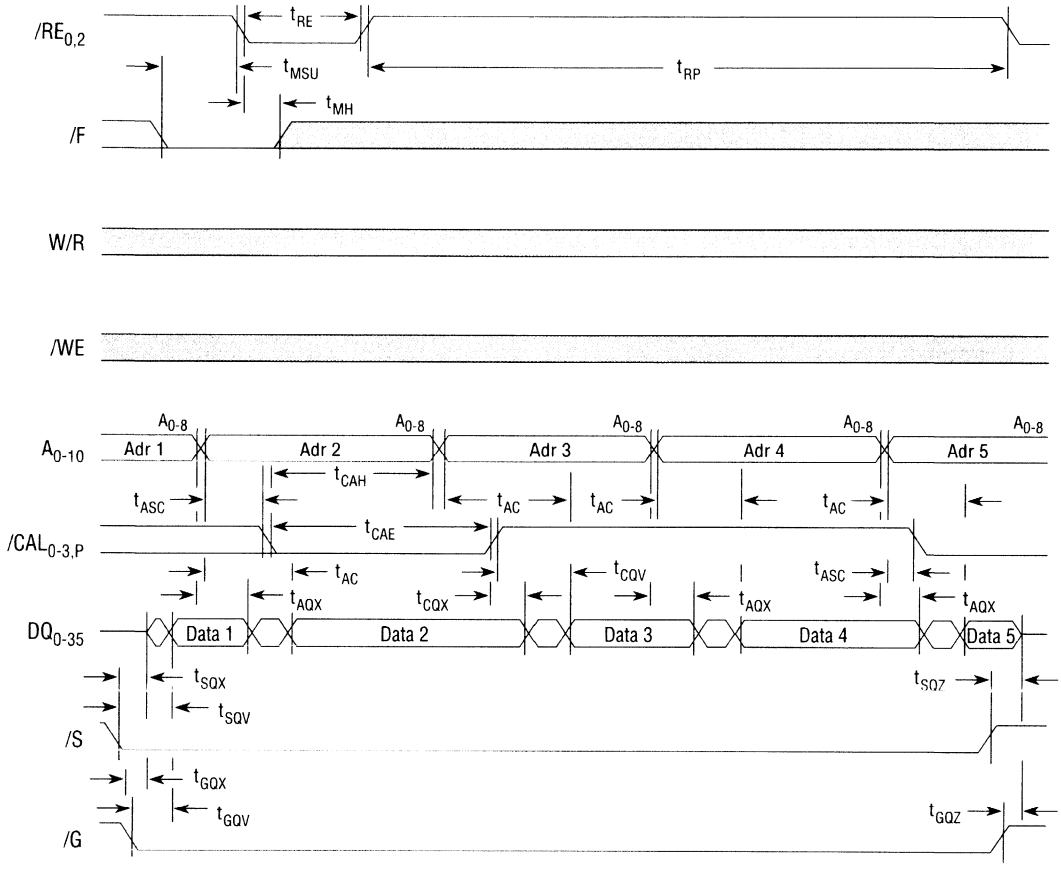


NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.

2. Two X4 EDRAM options are available, one with write-per-bit (DM2212) and one without write-per-bit (DM2202).

3. Write-per-bit waveform applies to parity bits only ($DQ_{8,17,26,35}$).

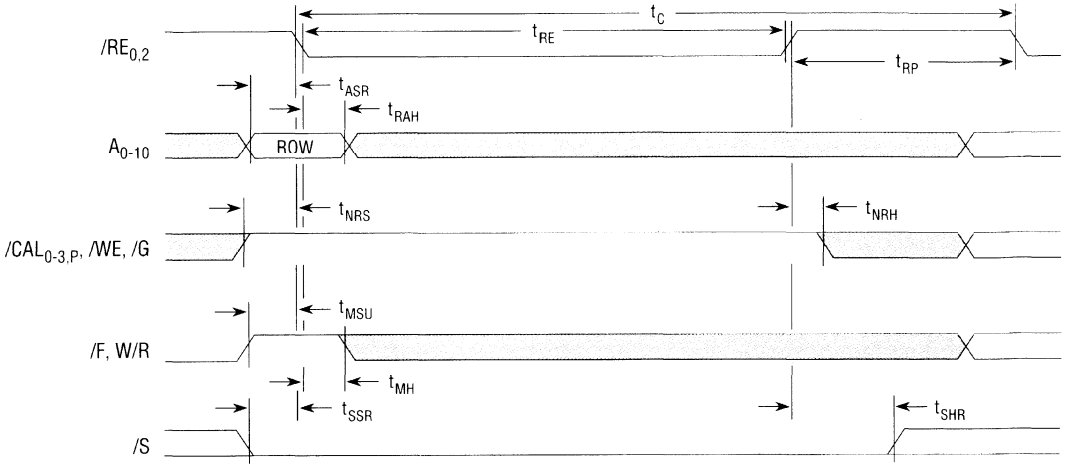
/F Refresh (Including "CAS Before RAS") with Page Mode and Static Column Cache Reads



NOTES: 1. During /F refresh cycles, /S is a don't care unless cache reads are performed. For cache reads, /S must be low.

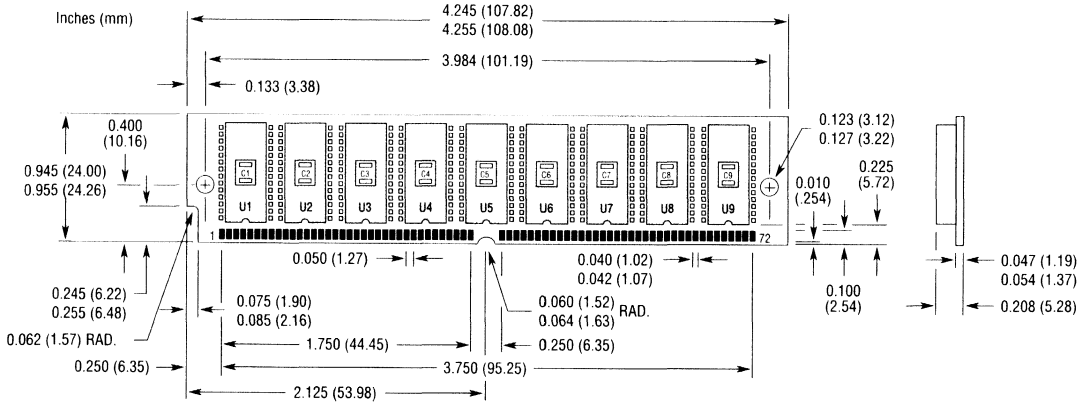
2. If /CAL is low when /RE falls, a "CAS before RAS" type refresh occurs.

/RE-Only Refresh



NOTES: 1. All binary combinations of $A_{0\text{-}9}$ must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

Mechanical Data
72 Pin SIMM Module



U1-U4, U6-U9 — Ramtron DM2202J-XX, 1M x 4 EDRAMs, 300 Mil SOJ
U5 — Ramtron DM2212J-XX, 1M x 4 EDRAM with Write-Per-Bit (Not present on DM 1M32SJ)
C1-C9 — 0.22µF Chip Capacitors
Socket — Molex 78441-7202 or Equivalent

Part Numbering System

DM1M36SJ - 15

- **Access Time from Cache in Nanoseconds**
  - 15ns
  - 20ns
- **Packaging System**
  - J = 300 Mil, Plastic SOJ
- **Memory Module Configuration**
  - S = SIMM
- **I/O Width (Including Parity)**
  - 32 = 32 Bits
  - 36 = 36 Bits
- **Memory Depth (Megabits)**
- **Dynamic Memory**

DM2M36SJ/DM2M32SJ
2Mbx36/2Mbx32 Enhanced DRAM SIMM

Product Specification

Features

- 4Kbyte SRAM Cache Memory for 15ns Random Reads Within a Page
- Fast DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- Simple On-chip Page Caching Control Allows DRAM-like System Architecture and Compatibility
- 4Kbyte Wide DRAM to SRAM Bus for 117 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge Cycles
- Hidden Refresh or /CAS Before /RAS Type Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- Compatibility with JEDEC 2M x 36 DRAM SIMM Configuration Allows Performance Upgrade in System

Description

The Ramtron 8Mb enhanced DRAM SIMM module provides a single memory module solution for the main memory or local memory of fast PCs, workstations, servers, and other high performance systems. Due to its fast 15ns cache row register, the EDRAM memory module supports zero-wait-state burst read operations at up to 40MHz bus rates in a non-interleave configuration and >66MHz bus rates with a two-way interleave configuration.

On-chip write posting and fast page mode operation supports 15ns write and burst write operations. On a cache miss, the fast DRAM array reloads the entire 2Kbyte cache over a 2Kbyte-wide bus in 35ns for an effective bandwidth of 58 Gbytes/sec. This means very low latency and fewer wait states on a cache miss than a non-integrated cache/DRAM solution. The JEDEC compatible 72-bit SIMM configuration allows a single memory controller to be designed to support either JEDEC slow DRAMs or high speed EDRAMs to provide a simple upgrade path to higher system performance.

Architecture

The DM2M36SJ achieves 2Mb x 36 density by mounting 18 1M x 4 EDRAMs, packaged in 28-pin plastic SOJ packages, on both sides of the multi-layer substrate. Sixteen DM2202 and two DM2212 devices provide data and parity storage. The DM2M32SJ contains 16 DM2202 devices for data only and parity memory is not included.

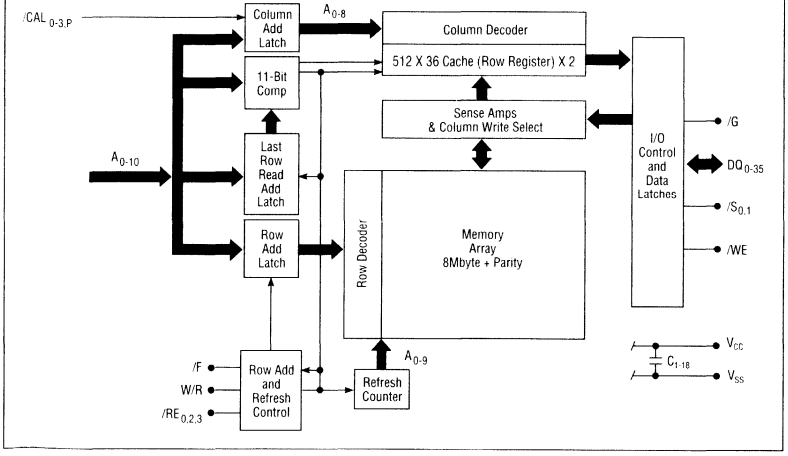
The EDRAM memory module architecture is very similar to a standard 8Mb DRAM module with the addition of an integrated cache and on-chip control which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the on-chip comparator detects a page hit, only the SRAM is accessed and data is available in 15ns from column address. When a page read miss is detected, the entire new DRAM row is loaded into the cache and data is available at the output all within 35ns from row enable. Subsequent reads within the page (burst reads or random reads) will continue at 15ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

Memory writes are internally posted in 15ns and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 15ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance

Functional Diagram



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without any significant increase in die size over standard slow DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address changes. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ($t_{RAH} + t_{ASC}$ for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 15ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	A_{0-10}	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	↓	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time t_{AC} after the column address is setup to /CAL.

Function	/S	/G	/CAL	A_{0-8}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

Write-Per-Bit Operation

The DM2M36SJ EDRAM SIMM provides a write-per-bit capability to selectively modify individual parity bits ($DQ_{8,17,26,35}$) for byte write operations. The parity device (DM2212) is selected via $/CAL_P$. Data bits do not require or support write-per-bit capability. Byte write selection to non-parity bits is accomplished via $/CAL_{0-3}$. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F type refresh cycle. When /F type refreshing is used, at least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled. In this case, the output remains disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_{0-9} must be sequenced every 64ms refresh period. A_{10} does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization.

Unallowed Mode

Read, write, or /RE only operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. If these techniques are used, the EDRAM will require only four control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], W/R, and /G). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

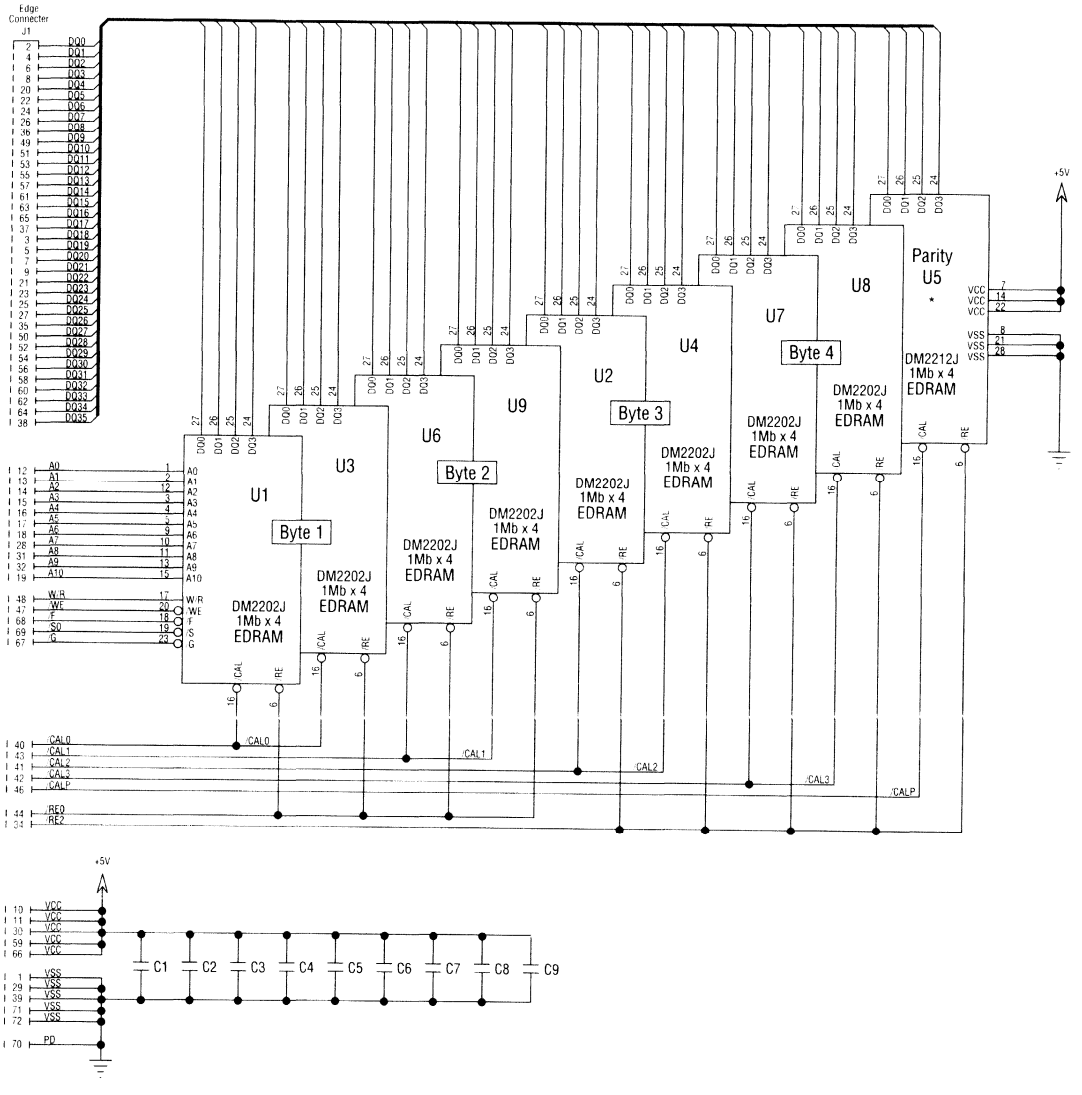
Pinout

Pin No.	Function	Interconnect (Component Pin)	Organization
1	GND	C (8,21,28)	Ground
2	DQ_0	U1,10 (27)	Byte 1 I/O 1
3	DQ_{18}	U2,11 (24)	Byte 3 I/O 1
4	DQ_1	U1,10 (26)	Byte 1 I/O 2
5	DQ_{19}	U2,11 (25)	Byte 3 I/O 2
6	DQ_2	U1,10 (25)	Byte 1 I/O 3
7	DQ_{20}	U2,11 (26)	Byte 3 I/O 3
8	DQ_3	U1,10 (24)	Byte 1 I/O 4
9	DQ_{21}	U2,11 (27)	Byte 3 I/O 4
10	+5 Volts	C (7,14,22)	V_{CC}
11	+5 Volts	C (7,14,22)	V_{CC}
12	A_0	C (1)	Address
13	A_1	C (2)	Address
14	A_2	C (12)	Address
15	A_3	C (3)	Address
16	A_4	C (4)	Address
17	A_5	C (5)	Address
18	A_6	C (9)	Address
19	A_{10}	C (15)	Address
20	DQ_4	U3,12 (27)	Byte 1 I/O 5
21	DQ_{22}	U4,13 (24)	Byte 3 I/O 5
22	DQ_5	U3,12 (26)	Byte 1 I/O 6
23	DQ_{23}	U4,13 (25)	Byte 3 I/O 6
24	DQ_6	U3,12 (25)	Byte 1 I/O 7
25	DQ_{24}	U4,13 (26)	Byte 3 I/O 7
26	DQ_7	U3,12 (24)	Byte 1 I/O 8
27	DQ_{25}	U4,13 (27)	Byte 3 I/O 8
28	A_7	C (10)	Address
29	GND	C (8,21,28)	Ground
30	+5 Volts	C (7,14,22)	V_{CC}
31	A_8	C (11)	Address
32	A_9	C (13)	Address
33	$/RE_3$	U10-18 (6)	Bank 1 Row Enable
34	$/RE_2$	U2,4,5,7,8 (6)	Bank 0 Row Enable (Bytes 3,4, Parity)
35	DQ_{26}*	U5,14 (27)	Parity I/O for Byte 3
36	DQ_8*	U5,14 (26)	Parity I/O for Byte 1
37	DQ_{17}*	U5,14 (25)	Parity I/O for Byte 2
38	DQ_{35}*	U5,14 (24)	Parity I/O for Byte 4
39	GND	C (8,21,28)	Ground
40	$/CAL_0$	U1,3,10,12 (16)	Byte 1 Column Address Latch
41	$/CAL_2$	U2,4,11,13 (16)	Byte 3 Column Address Latch
42	$/CAL_3$	U7,8,16,17 (16)	Byte 4 Column Address Latch
43	$/CAL_1$	U6,9,15,18 (16)	Byte 2 Column Address Latch
44	$/RE_0$	U1,3,6,9 (6)	Bank 0 Row Enable (Bytes 1,2)
45	$/S_1$	U10-18 (19)	Chip Select Bank 1
46	$/CAL_P$*	U5,14 (16)	Parity Column Address Latch
47	/WE	C (20)	Write Enable
48	W/R	C (17)	W/R Mode Control
49	DQ_9	U6,15 (27)	Byte 2 I/O 1
50	DQ_{27}	U7,16 (27)	Byte 4 I/O 1
51	DQ_{10}	U6,15 (26)	Byte 2 I/O 2
52	DQ_{28}	U7,16 (26)	Byte 4 I/O 2
53	DQ_{11}	U6,15 (25)	Byte 2 I/O 3
54	DQ_{29}	U7,16 (25)	Byte 4 I/O 3
55	DQ_{12}	U6,15 (24)	Byte 2 I/O 4
56	DQ_{30}	U7,16 (24)	Byte 4 I/O 4
57	DQ_{13}	U9,18 (24)	Byte 2 I/O 5
58	DQ_{31}	U8,17 (24)	Byte 4 I/O 5
59	+5 Volts	C (7,14,22)	V_{CC}
60	DQ_{32}	U8,17 (26)	Byte 4 I/O 6
61	DQ_{14}	U9,18 (25)	Byte 2 I/O 6
62	DQ_{33}	U8,17 (25)	Byte 4 I/O 7
63	DQ_{15}	U9,18 (26)	Byte 2 I/O 7
64	DQ_{34}	U8,17 (24)	Byte 4 I/O 8
65	DQ_{16}	U9,18 (27)	Byte 2 I/O 8
66	+5 Volts	C (7,14,22)	V_{CC}
67	/G	C (23)	Output Enable
68	/F	C (18)	Refresh Mode Control
69	$/S_0$	U1-9 (19)	Chip Select Bank 0
70	PD	Signal GND	Presence Detect
71	GND	C (8,21,28)	Ground
72	GND	C (8,21,28)	Ground

C = Common to All Memory Chips. U1 = Chip 1, etc.

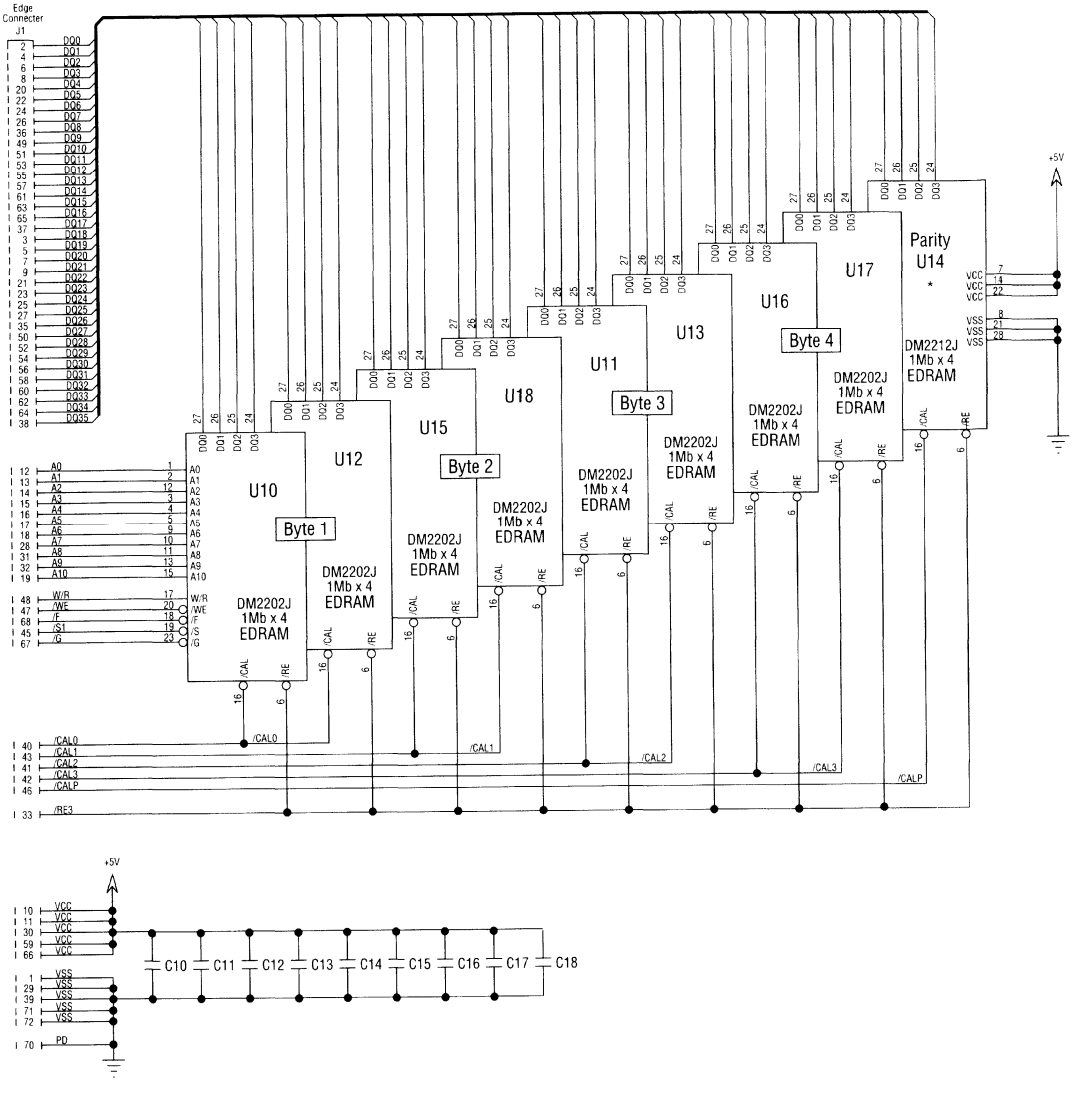
*No Connect for DM2M32SJ

Interconnect Diagram — Bank 0 (Components Mounted on Front Side)



*DM2212 is not present on the DM2M32SJ.

Interconnect Diagram — Bank 1 (Components Mounted on Back Side)



*DM2212 is not present on the DM2M32SJ.

Pin Descriptions

/$RE_{0,2,3}$ — Row Enable

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

/$CAL_{0-3,P}$ — Column Address Latch

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pin during read operations.

/$S_{0,1}$ — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition; read and write cycles cannot be executed while /S is high. /S must remain active throughout any read or write operation. Only the /F refresh operation can be executed when /S is high.

DQ_{0-35} — Data Input/Output

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2212 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 9-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

These inputs are connected to the power supply ground connection.

2

Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current (I_{OUT})	50mA*

* One output at a time per device; short duration

Capacitance

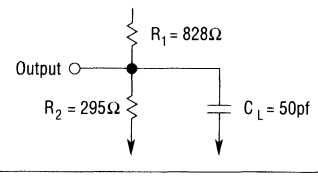
Description	Max*	Pins
Input Capacitance	130/136pf	A_{0-9}
Input Capacitance	165/180pf	A_{10}, W/R, /WE, /F
Input Capacitance	97/100pf	/S_0, /S_1
Input Capacitance	52/55pf	/RE_0
Input Capacitance	55/65pf	/RE_2
Input Capacitance	92/92pf	/RE_3
Input Capacitance	62/62pf	/G
Input Capacitance	52/55pf	/CAL_{0-3}
Input Capacitance	32pf	/CAL_P
I/O Capacitance	16pf	DQ_{0-35}

* DM2M32SJ/DM2M36SJ, respectively

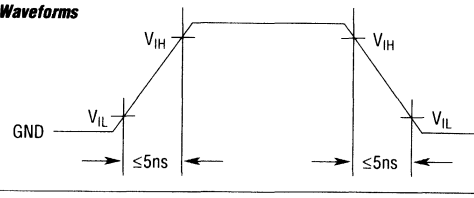
AC Test Load and Waveforms

V_{IN} Timing Reference Point at V_{IL} and V_{IH}

Load Circuit



Input Waveforms



Electrical Characteristics

(T_A = 0 - 70°C)

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	-10µA	10µA	$0V \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-10µA	10µA	$0V \le V_{IN}$, $0V \le V_{OUT} \le 5.5V$

Operating Current — DM2M32SJ

Symbol	Operating Current	33MHz Typ[1]	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	880mA	1800mA	1440mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	520mA	1160mA	920mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	440mA	880mA	720mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	1080mA	1520mA	1200mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	400mA	1080mA	840mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	16mA	16mA	16mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	240mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

Operating Current — DM2M36SJ

Symbol	Operating Current	33MHz Typ[1]	-15 Max	-20 Max	Test Condition	Notes
I_{CC1}	Random Read	990mA	2025mA	1620mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	585mA	1305mA	1035mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	495mA	990mA	810mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	1215mA	1710mA	1350mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	450mA	1215mA	945mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	18mA	18mA	18mA	All Control Inputs Stable ≥ V_{CC} - 0.2V	
I_{CCT}	Average Typical Operating Current	270mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. In this typical example, page mode and random reads refer to page burst hits and misses. Writes are two clock cycle random and page mode writes. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.

(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

Discrete devices have been tested from 4.7V to 5.3V V_{CC} and to 75°C to guarantee SIMM specifications. (V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50pf)

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{AC}[1]	Column Address Access Time		15		20	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
t_{AQX}	Column Address Change to Output Data Invalid	5		5		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		6		ns
t_C	Row Enable Cycle Time	65		85		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
t_{CA}	Address Cycle Time (Cache Hits)	15		20		ns
t_{CAE}	Column Address Latch Active Time	6		7		ns
t_{CAH}	Column Address Hold Time	0		1		ns
t_{CDR}[2]	Column Address Delay from /RE Low, After /CAL Assertion in a Write Hit Cycle	35		45		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		7		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-1		-1		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		17		20	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid	5		5		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		6		ns
t_{CWL}	/WE Low to /CAL Inactive	5		7		ns
t_{DH}	Data Input Hold Time	0		1		ns
t_{DMH}	Mask Hold Time From Row Enable (Write-Per-Bit)	1.5		2		ns
t_{DMS}	Mask Setup Time to Row Enable (Write-Per-Bit)	5		6		ns
t_{DS}	Data Input Setup Time	5		6		ns
t_{GQV}[1]	Output Enable Access Time		5		6	ns
t_{GQX}[3,4]	Output Enable to Output Drive Time	0	5	0	6	ns
t_{GQZ}[5,6]	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	6	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		1		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		6		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
t_{PC}	Column Address Latch Cycle Time	15		20		ns
t_{RAC}[1]	Row Enable Access Time, On a Cache Miss		35		45	ns
t_{RAC1}[1]	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		17		22	ns
t_{RAC2}[1,7]	Row Enable Access Time for a Cache Write Hit		35		45	ns
t_{RAH}	Row Address Hold Time	1.5		2		ns
t_{RE}	Row Enable Active Time	35	100000	45	100000	ns

Switching Characteristics (continued)

Discrete devices have been tested from 4.7V to 5.3V V_{CC} and to 75°C to guarantee SIMM specifications. (V_{CC} = 5V ± 5%, T_A = 0 to 70°C, C_L = 50pf)

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	10		13		ns
t_{RP}(8)	Row Precharge Time	25		32		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		1		ns
t_{RSH}	Last Write Address Latch to End of Write	15		20		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	40		51		ns
t_{RWL}	Last Write Enable to End of Write	15		20		ns
t_{SC}	Column Address Cycle Time	15		20		ns
t_{SHR}	Select Hold From Row Enable	0		1		ns
t_{SQV}(1)	Chip Select Access Time		15		20	ns
t_{SQX}(3,4)	Output Turn-On From Select Low	0	15	0	20	ns
t_{SQZ}(5,6)	Output Turn-Off From Chip Select	0	10	0	13	ns
t_{SSR}	Select Setup Time to Row Enable	5		6		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	15		20		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
t_{WHR}(9)	Write Enable Hold After /RE	0		1		ns
t_{WI}	Write Enable Inactive Time	5		7		ns
t_{WP}	Write Enable Active Time	5		7		ns
t_{WQV}(1)	Data Valid From Write Enable High		15		20	ns
t_{WQX}(3,6)	Data Output Turn-On From Write Enable High	0	15	0	20	ns
t_{WQZ}(4,5)	Data Turn-Off From Write Enable Low	0	15	0	20	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Cache Miss)		15		20	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Column Address is Ignored Prior to t_{CDR} for This Specific Cycle

(3) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(4) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

(5) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

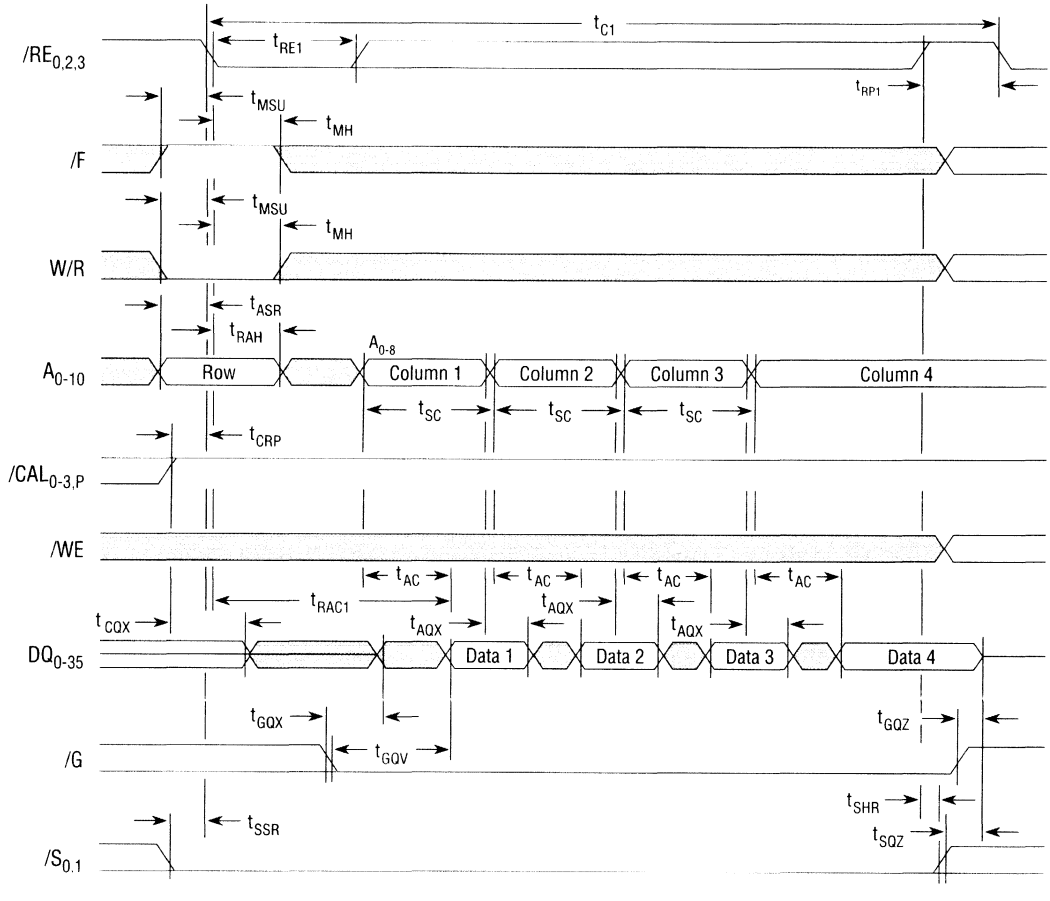
(6) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{III} on Input Control Signal

(7) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

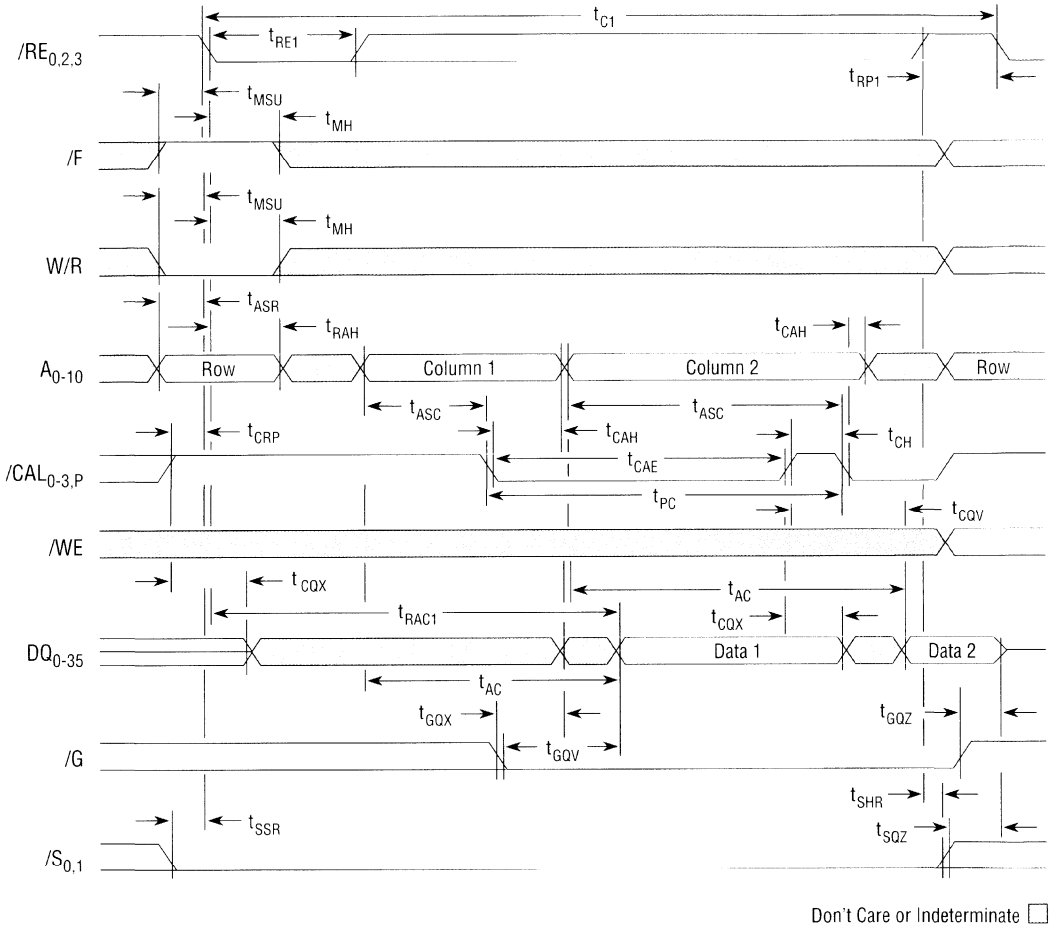
(8) For Back-to-Back /F Refreshes, t_{RP} = 40ns. For Non-consecutive /F Refreshes, t_{RP} = 25ns and 32ns Respectively

(9) For Write-Per-Bit Devices, t_{WHR} is Limited By Data Input Setup Time, t_{DS}

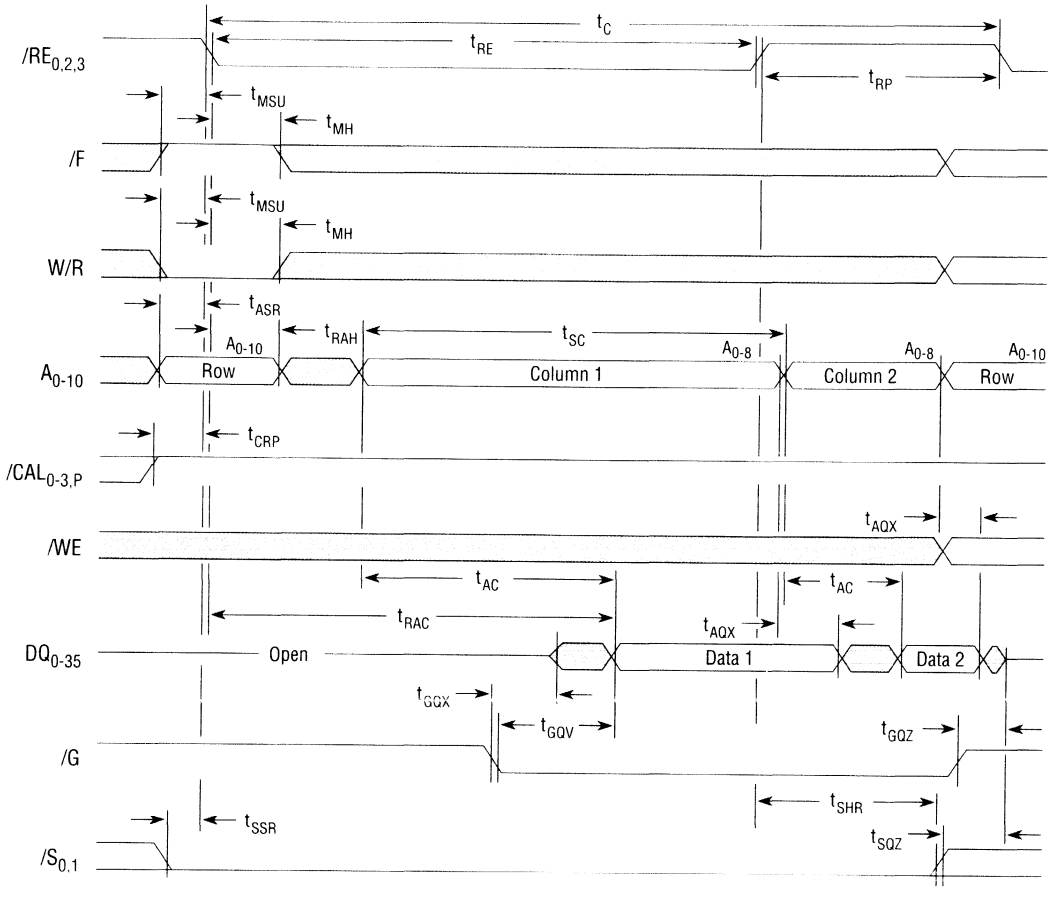
/RE Active Cache Read Hit (Static Column Mode)



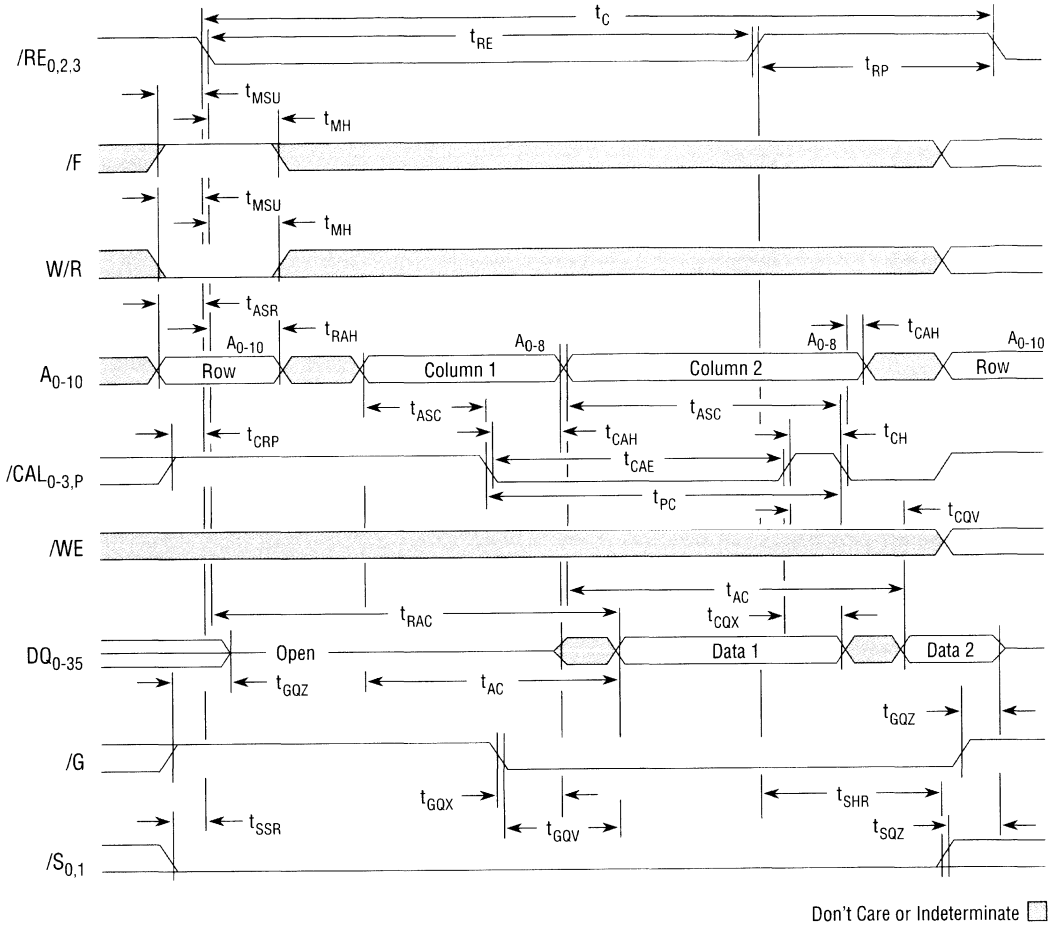
/RE Active Cache Read Hit (Page Mode)



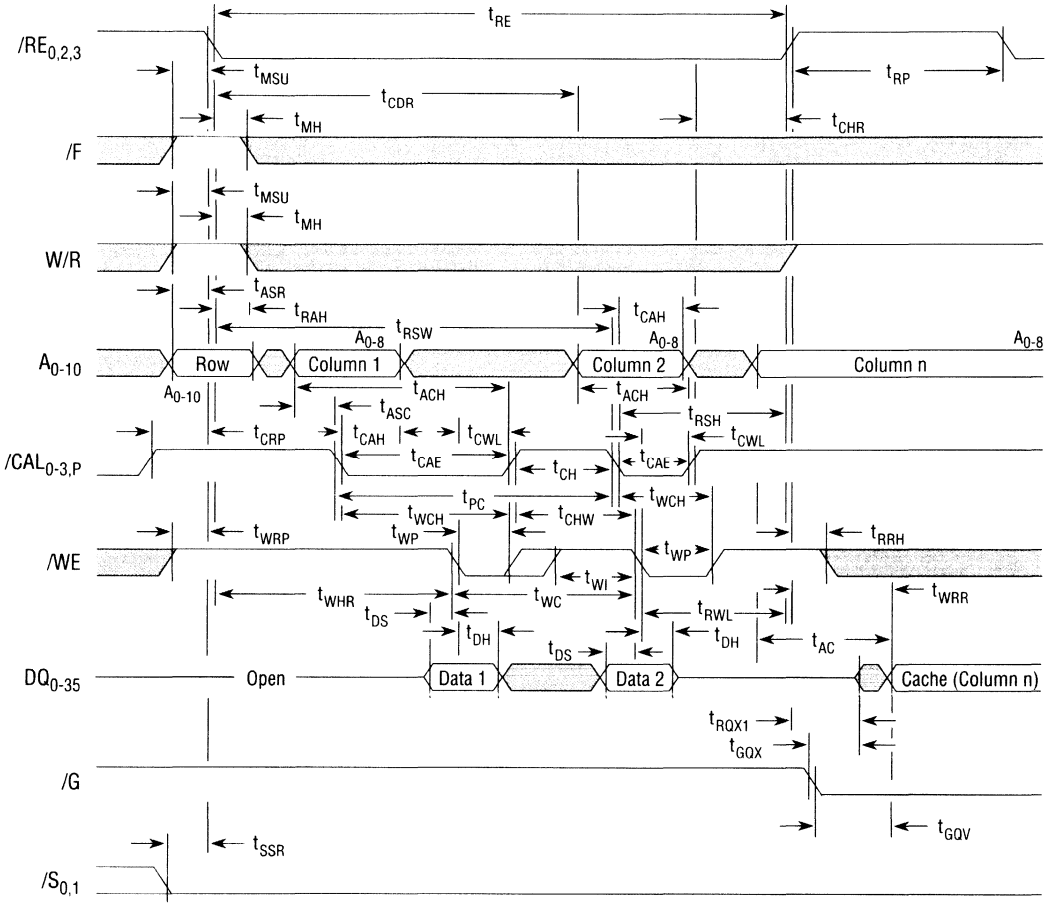
/RE Active Cache Read Miss (Static Column Mode)



/RE Active Cache Read Miss (Page Mode)



Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



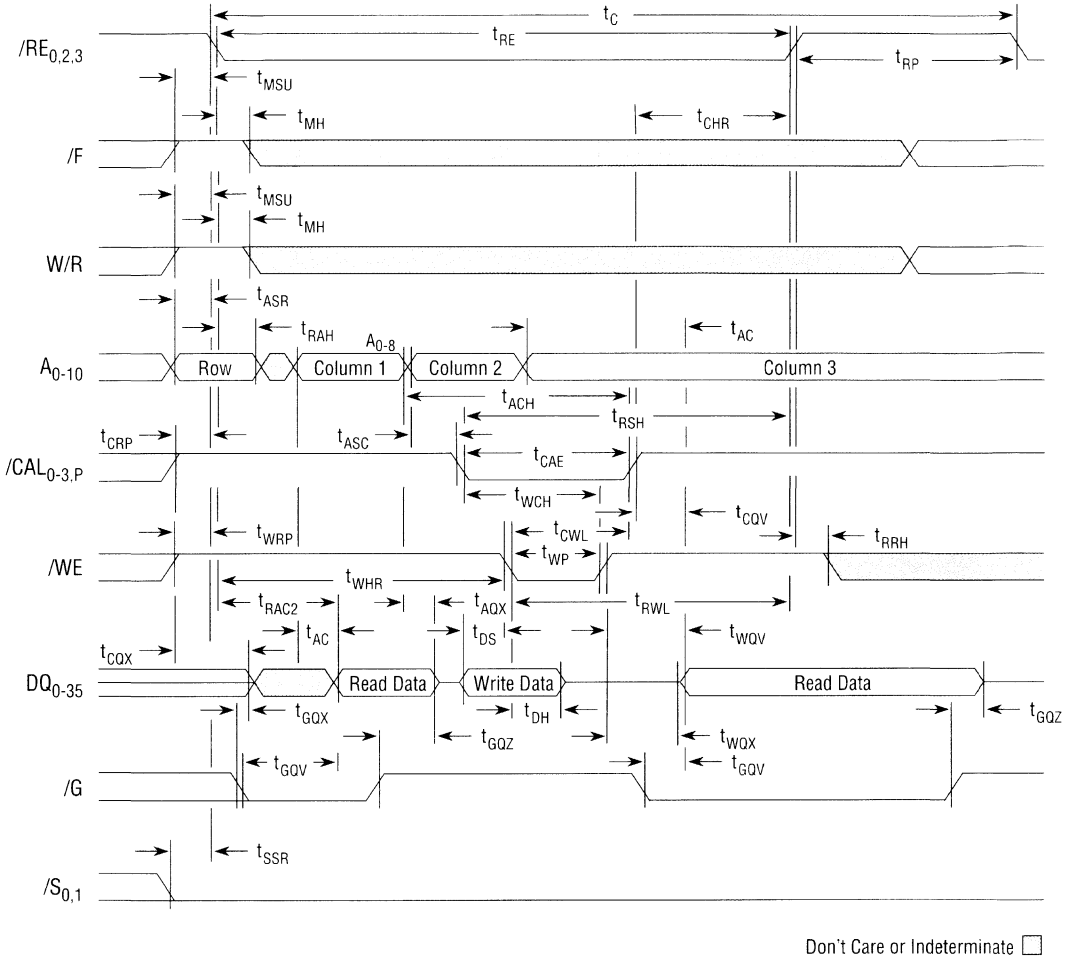
NOTES: 1. Parity bits $DQ_{8,17,26,35}$ must have mask provided at falling edge of /RE.

2. On a write miss cycle that is directly followed by a read hit, W/R must be high simultaneously or before /RE goes high.

3. /G becomes a don't care after t_{RGX} during a write miss.

4. t_{CDR} only applies if /CAL falls prior to t_{RAC2} timing interval.

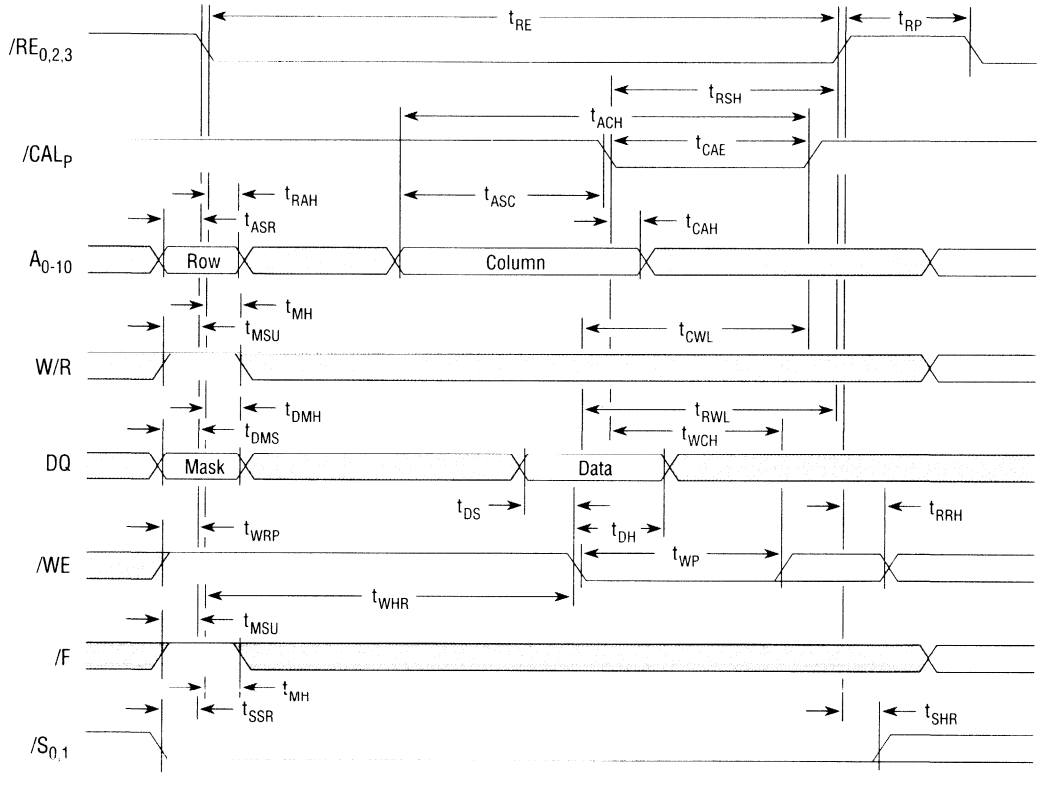
Page Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address 1 equals column address 2, then a read-modify-write cycle is performed.

2. Parity bits $DQ_{8,17,26,35}$ must have mask provided at falling edge of /RE.

Write-Per-Bit Cycle (/G = High)



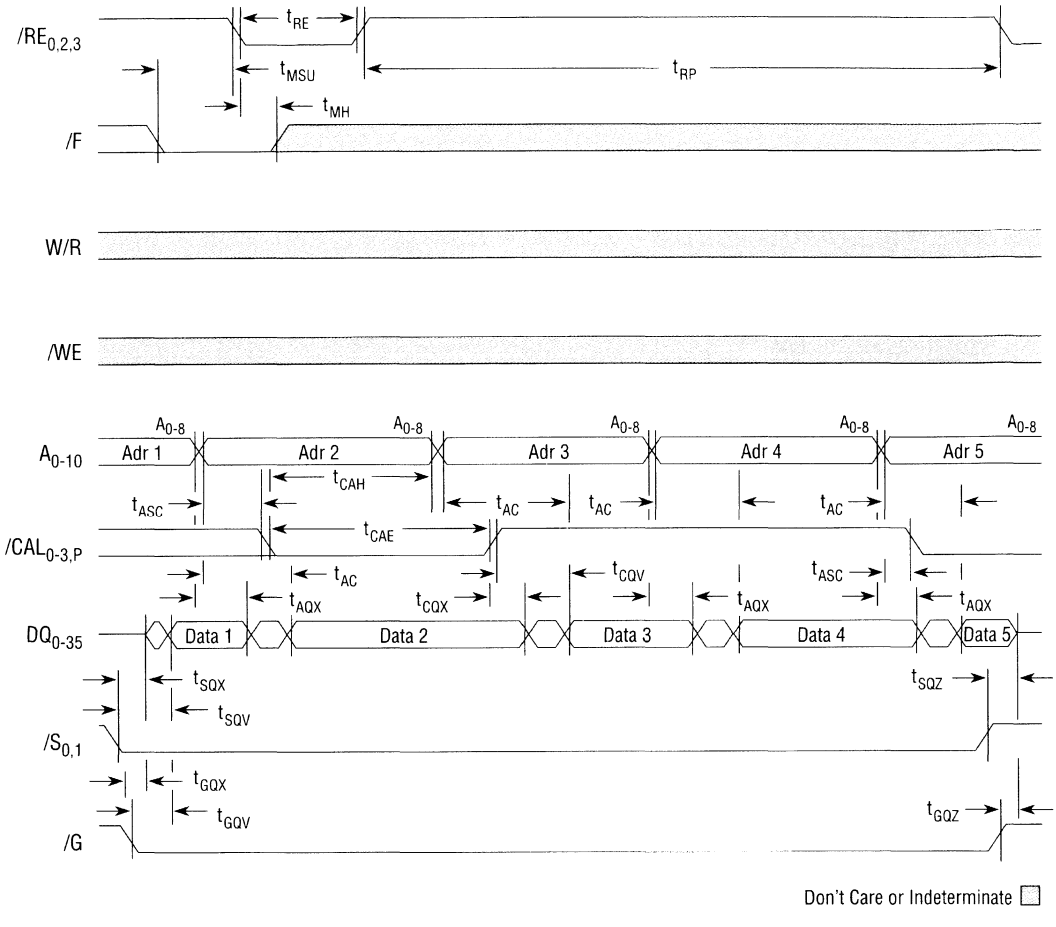
Don't Care or Indeterminate ☐

NOTES: 1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.

2. Two X4 EDRAM options are available, one with write-per-bit (DM2212) and one without write-per-bit (DM2202).

3. Write-per-bit waveform applies to parity bits only ($DQ_{8,17,26,35}$).

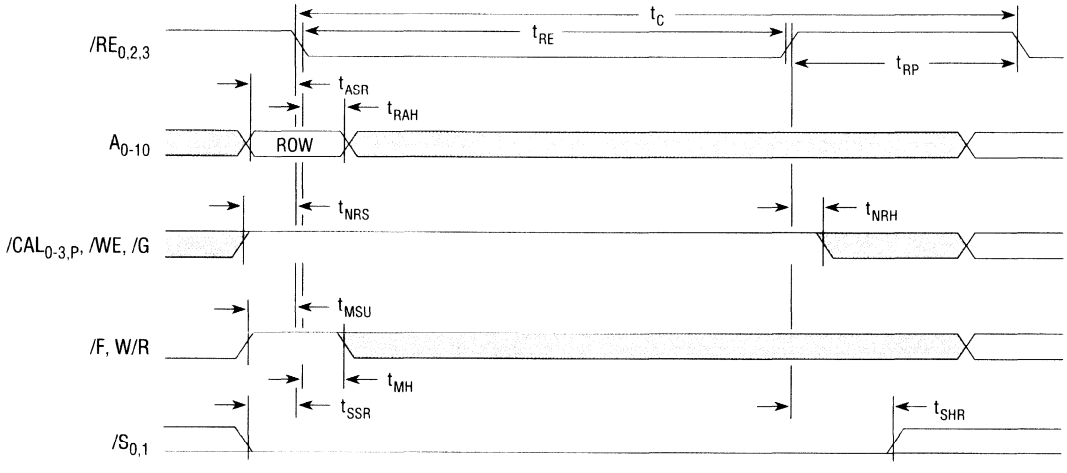
/F Refresh (Including "CAS Before RAS") with Page Mode and Static Column Cache Reads



NOTES: 1. During /F refresh cycles, /S is a don't care unless cache reads are performed. For cache reads, /S must be low.

2. If /CAL is low when /RE falls, a "CAS before RAS" type refresh occurs.

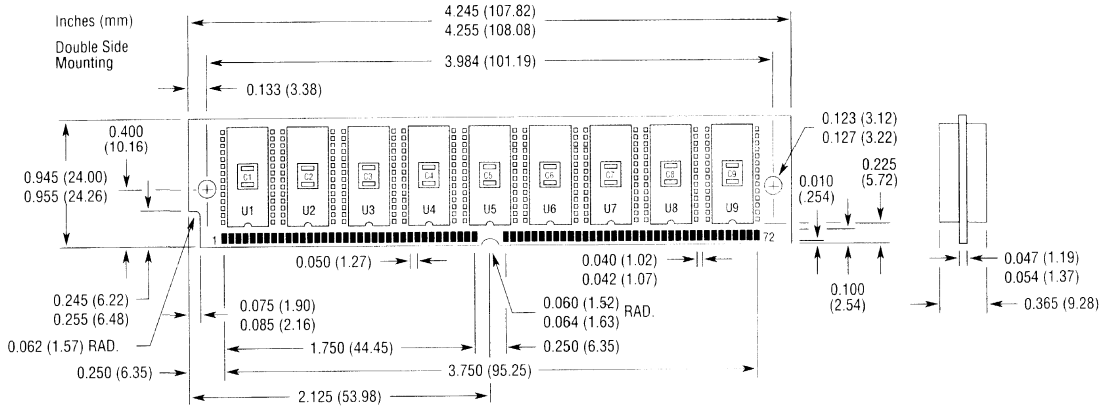
/RE-Only Refresh



NOTES: 1. All binary combinations of $A_{0\text{-}9}$ must be refreshed every 64ms interval. A_{10} does not have to be cycled, but must remain valid during row address setup and hold times.

2

Mechanical Data
72 Pin SIMM Module



U1-U4, U6-U9, U10-U13, U15-U17 — Ramtron DM2202J-XX, 1M x 4 EDRAMs, 300 Mil SOJ
U5, U14 — Ramtron DM2212J-XX, 1M x 4 EDRAM with Write-Per-Bit (Not present on DM2M32SJ)
C1-C18 — 0.22µF Chip Capacitors
Socket — Molex 78441-7202 or Equivalent

Part Numbering System

DM2M36SJ - 15

Access Time from Cache in Nanoseconds
15ns
20ns

Packaging System
J = 300 Mil, Plastic SOJ

Memory Module Configuration
S = SIMM

I/O Width (Including Parity)
32 = 32 Bits
36 = 36 Bits
40 = 40 Bits

Memory Depth (Megabits)
1M
2M
4M

Dynamic Memory

EDRAM Design Hints

Application Note

This application note is a collection of design suggestions based upon common errors made during the development of EDRAM systems.

Initialization

To assure reliable operation of the EDRAM, please initialize promptly on power-up. This initialization requires eight /F refresh cycles and two /RE active read cycles per bank to different row addresses. The /F refresh cycles would normally be performed while power-up reset is active. The read cycles would typically be executed as part of a system startup program. It will not be possible to read data properly without initialization.

End Write Cycles With /CAL High

Unlike a standard DRAM, the EDRAM t_{CHR} specification requires that /CAL be brought high before /RE when ending a write cycle to assure proper write termination.

W/R Mode Operation

It has been found that the W/R mode signal must be high for both falling and rising edges of /RE during write miss cycles. As a matter of practice, please make sure W/R is high during the entire /RE active period for reliable operation.

Unallowed Mode

The EDRAM does not disable all logic when the /S chip select is disabled. As a result, /RE should never be clocked in read or write mode when /S is disabled. The EDRAM cache control logic is corrupted when this operation occurs.

Power Supply

High speed EDRAM operation can generate high transient power supply currents. Adequate decoupling (typically 0.22µF per chip near power pins) and a low impedance power and ground bus are necessary to prevent the power supply voltage from dropping below the +4.75 volt minimum specification during transients. Wire wrap boards will not normally provide an adequate power bus. Please use a well designed PC board for both prototype and production systems.

Air Flow

The EDRAM, like other high performance products, can dissipate a significant amount of heat when operated at its maximum random duty cycle (i.e., 65ns /RE cycle time). The heat generated by the EDRAM, the microprocessor, and other high performance devices can lead to unreliable operation if no airflow is provided. Since the microprocessor, memory controller, and memory are all in the critical timing path, additional airflow for all three may sometimes be advisable. Please use our power application note to better understand the expected operation current for your system. EDRAM power can be reduced by using the /S chip select to place devices in their low power mode when not in use and by using the /RE inactive cache access mode to minimize the /RE duty cycle. In this mode of operation, air flow is not typically required for the memory. The microprocessor and controller, however, may still benefit from cooling efforts.

Estimating EDRAM Operating Power

Application Note

Introduction

The Ramtron enhanced DRAM combines the functions of a fast 35ns DRAM, 15ns SRAM cache memory, 256-byte wide DRAM to SRAM bus, and write posting register on a single chip. As a result, it provides a much higher level of integration, faster performance, and lower power than an equivalent system built using a secondary SRAM cache, cache controller, two-way or four-way interleave DRAM, and DRAM controller.

Like DRAMs, EDRAM power consumption is dependent on cycle time and mode of operation. It becomes necessary to understand a number of important statistics about the exact system operation to properly estimate the operating power. This application note will summarize the characterization of EDRAM power under different operating conditions and frequencies. From these results, equations are developed to estimate EDRAM current at different clock rates. A model for EDRAM operating power is then developed based upon Intel 486 bus activity assumptions. Finally, the EDRAM peak, operating, and standby currents are estimated for the 25MHz and 33MHz bus rates typical of most high performance 486DX and 486DX2 systems today. Using these examples, it should be easy to develop models of operating power in other types of computer systems.

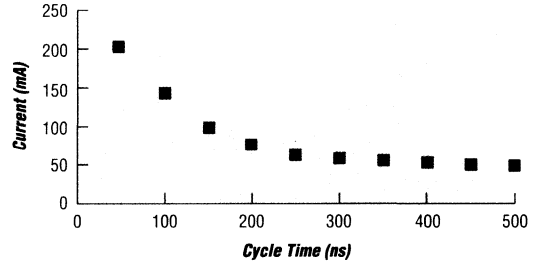
EDRAM Supply Current Characterization Results

Ramtron has characterized a number of operating modes over a range of cycle times. Operating currents shown include random read and write current, page mode read and write current, and static column read current. Both CMOS and TTL interface characterizations are included. All current measurements were taken at worst case temperature of -5°C.

EDRAM Standby Current — The EDRAM is specified at 1mA standby current with CMOS levels and characterized at 16mA standby current (worst case) with TTL levels. Operating at TTL interface levels increases the standby current significantly since the TTL input buffers tend to operate close to their input threshold resulting in higher current flow in the buffer. Since actual TTL drivers never operate at specification minimums (noise margins are built into the specifications), actual TTL standby current will be significantly lower than specified.

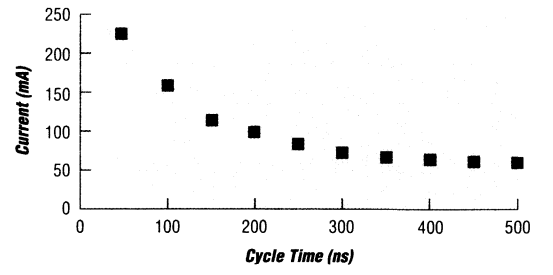
Random Read Operating Current — The EDRAM can operate at random read cycle times from 65ns minimum to 62,400ns maximum (refresh rate). If the row address specified is always different, a page miss will occur and the EDRAM will load a new row of data into the on-chip SRAM cache on each cycle. During characterization, we measured the read miss operating current at three cycle times (65, 85, and 325ns). From this data, we developed a simple formula to fit the data. This formula can then be used to estimate the current at any cycle time within the operating range. The random read current with CMOS operating levels is shown in Figure 1. The formula for estimating current is (65ns/operating cycle time * 180) + 25. From this formula, we see that the static read current with /S enabled is about 25mA and the maximum read current at 65ns cycle time is 205mA.

Figure 1. Random Read Current — CMOS Levels



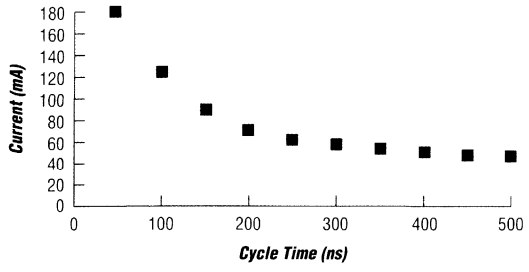
The random read current for TTL levels is shown in Figure 2. The formula for estimating current is (65/cycle time * 187) + 38. Static read current with /S enabled is about 38mA and maximum read current at 65ns is 225mA. The difference in current between CMOS and TTL operation is roughly the same input leakage current difference seen in the static current specification.

Figure 2. Random Read Current — TTL Levels



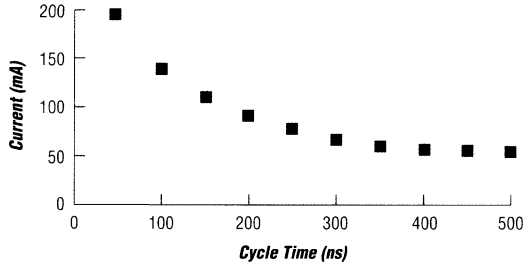
Random Write Current — The random write current was characterized at the same 65ns, 85ns, and 325ns cycle times and a formula was developed to fit the data. The random write current at CMOS levels is shown in Figure 3. The formula for estimating current is (65/cycle time * 157) + 22.

Figure 3. Random Write Current — CMOS Levels



The random write current at TTL levels is shown in Figure 4. The formula for estimating current is (65/cycle time * 160) + 36.

Figure 4. Random Write Current — TTL Levels



Page Mode Write Current — Page mode write current was characterized by measuring write cycles with /CAL cycling at 35ns, 40ns, and 200ns cycle times. From this data, we fit curves which allow write current to be estimated at the maximum 15ns rate and at slower cycle times. The page mode write current at CMOS levels is shown in Figure 5. The formula for estimating current is (35/cycle time * 46) + 23.

Figure 5. Page Mode Write Current — CMOS Levels

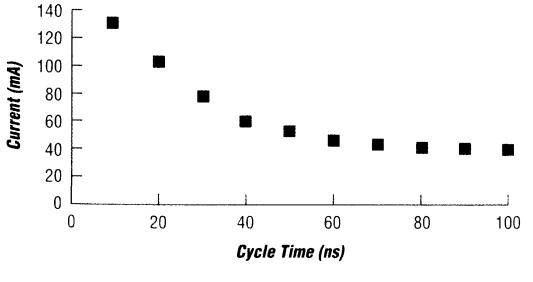
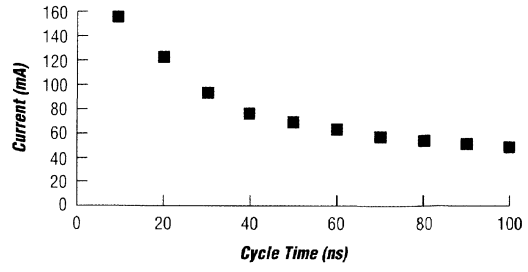


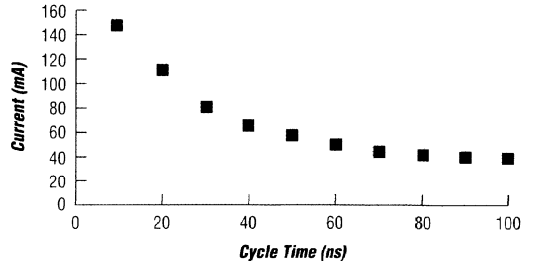
Figure 6. Page Mode Write Current — TTL Levels



The page mode write current with TTL levels is shown in Figure 6. The formula for estimating current is (35/cycle time * 50) + 36.

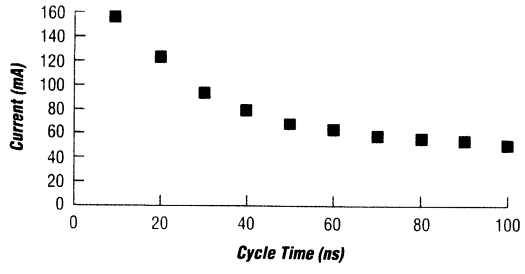
Page Mode + Static Column Read Current — The read current was characterized at 35ns, 40ns, and 100ns cycle times for both page mode (clocked /CAL) and static column mode (/CAL high). Using this data, a formula for each current was fit to the data. This allows us to estimate current at the maximum cycle time of 15ns as well as other cycle times. The read current for page mode operation and CMOS levels is shown in Figure 7. The formula for estimating current is (35/cycle time * 54) + 17.

Figure 7. Page Mode Read Current — CMOS Levels



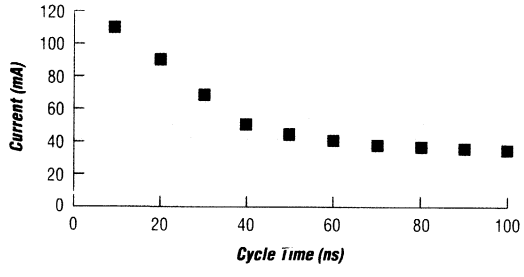
The read current for page mode and TTL levels is shown in Figure 8. The formula for estimating current is (35/cycle time * 52) + 32.

Figure 8. Page Mode Read Current — TTL Levels



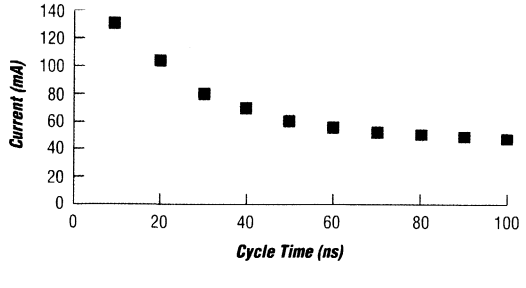
The read current for static column operation with CMOS levels is shown in Figure 9. The formula for estimating current is (35/cycle time * 39) + 18.

Figure 9. Static Column Read Current — CMOS Levels



The read current for static column operation at TTL levels is shown in Figure 10. The formula for estimating current is (35/cycle time * 41) + 29.

Figure 10. Static Column Read Current — TTL Levels



Calculating Actual EDRAM System Power Requirements

We can now develop an equation for estimating EDRAM power under different system operating conditions. We will use the Intel 486 local bus operation as the basis of this equation. Models could be easily developed for other processor bus structures using the same approach.

The main memory references on the Intel 486 local bus take the form of burst read and write cycles. Burst read cycles are used to refill the on-chip primary cache. Write cycles are the result of processor write throughs to the bus. Since the 486 system has a primary cache, the processor will execute a high percentage of read operations from the on-chip cache. This fact results in fairly low local bus utilization and a fairly balanced mix of read and write cycles. The following model will assume that the local bus is used only 33% of the time. I will assume that an equal mix of burst read and write cycles will occur and that 50% of burst read cycles will be burst read page hits (an 88% EDRAM cache hit rate).

The EDRAM will not operate at its maximum specified cycle times with the 486 processor. During burst read hit cycles, the EDRAM memory controller must generate EDRAM addresses and the cache data must be setup to the processor during each burst cycle. The cache is also idle during the initial T1 cycle which generates the burst starting address. During a burst read miss, the DRAM is accessed during the initial read cycle and then is idle while the remaining burst cycles are accessed from cache. As a result, the duty cycle of DRAM read/write and cache read cycles will vary by bus clock rate and memory reference type. The table below summarizes the effective cycle times of the DRAM and cache portions of the EDRAM for both 25MHz and 33MHz 486 bus operation.

Effective EDRAM Cycle Times

Clock Rate	EDRAM Mode	Burst Read Miss	Burst Read Hit	Write
25MHz	Random	240ns	N/A	80ns
25MHz	Page/Static Column	60ns	50ns	N/A
33MHz	Random	180ns	N/A	90ns
33MHz	Page/Static Column	45ns	37.5ns	N/A

Using these assumptions, we can develop a model for EDRAM operating current.

% bus idle time * standby current +
% bus active time * % burst reads * % burst read page misses * burst read miss current +
% bus active time * % burst reads * % burst read page hits * burst read hit current +
% bus active time * % writes * % random writes * random write current +
% bus active time * % writes * % page writes * page write current +
% refresh time * refresh current

Now let's work through an example calculation. First, we calculate the EDRAM maximum currents for each mode at 33MHz. Note that burst read miss current is calculated by averaging the random read current for the first three bus cycles and the static column read current for the last three bus cycles of the burst read miss cycle (3:1:1:1). The burst read hit current is calculated using the static column read current only.

Burst read miss current =
((65/90*180)+25) + ((35/30*39) + 18)/2 = 109mA
Burst read hit current = (35/37.5 * 39) + 18 = 54mA
Random write current = (65/90 * 157) + 22 = 132mA
Page write current = (35/60 * 46) + 23 = 50mA
Refresh current = (65/65 * 180) + 25 = 205mA

Now we can complete the operating current calculation for the bus utilization statistics stated earlier.

33MHz Operating Current =
66.9% (bus idle time) * 1mA (standby current) +
33% (bus active time) * 50% (burst reads) * 50% (burst read misses) * 109mA (burst read miss current) +
33% (bus active time) * 50% (burst reads) * 50% (burst read hits) * 54mA (burst read hit current) +
33% (bus active time) * 50% (writes) * 50% (random writes) * 132mA (random write current) +
33% (bus active time) * 50% (writes) * 50% (page mode writes) * 50mA (page mode write current) +
0.1% (refresh time) * 205mA (maximum refresh current) = 30mA

It is also useful to calculate the standby current of the EDRAM with periodic refresh since this defines the power of any unused EDRAM memory banks. This current can be calculated by setting bus idle time to 99.9%, bus active time to 0%, and refresh time to 0.1%.

The system designer will also want to calculate the peak read and peak write current at the specified clock rate so that the power supply design and power bussing can support the theoretical maximum power. These calculations are made by setting bus idle time to 0%, bus active time to 99.9%, and allowing 100% bus read misses or 100% write miss rates.

To summarize the different currents calculated at 33MHz, see Figure 11 below

We can now calculate the same current values for a 486 operating at 25MHz. These values are shown in Figure 12.

As we see from these calculations, the typical operating current for the EDRAM operating in a 486 system will be significantly below the EDRAM maximum datasheet power specifications and peak power requirements. For example, at 33MHz the typical power per EDRAM will be 30mA * 5.0 volts or 150 mW. All EDRAMs that are not active will be idling at 6mW. A DM1M36SJ EDRAM SIMM module would have a typical operating power of 1.35 watts and a standby power of 54mW.

Figure 11. EDRAM Current for 33MHz 486 Systems

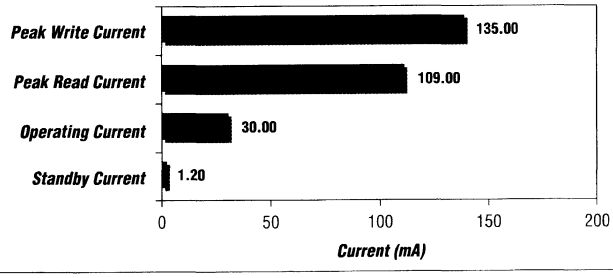
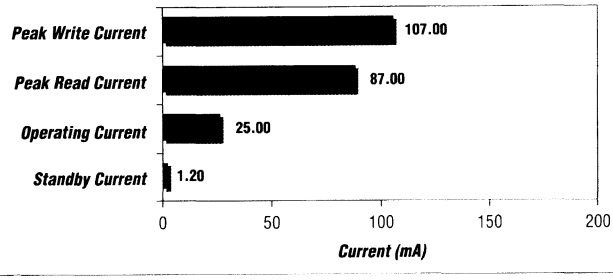


Figure 12. EDRAM Current for 25MHz 486 Systems



EDRAM Controller For 25MHz & 33MHz Intel i960CA/CF Microprocessors

Application Note

Summary

Ramtron's enhanced DRAM (EDRAM) memory is the ideal memory for high performance embedded control systems.

- No Wait States During Burst Read Hit
- Only One Wait State During Burst Read Miss and Burst Write Cycles
- Single Chip FPGA-based Controller Solution

Introduction

The Intel i960 family of 32-bit microprocessors is popular for high performance embedded control applications. The i960CA/CF processors are the highest performance members of this family. These processors use a 32-bit non-multiplexed bus which supports up to four word burst reads or writes. The bus supports pipelined operations and allows both internal and external insertion of wait states. The i960CA/CF processors are available in 16, 25, and 33MHz clock speed options.

Ramtron's EDRAM is the ideal main memory component to support the i960CA/CF processors at 25 and 33MHz clock rates. Its fast 15ns read access time allows all read cycles which hit the on-chip cache to be performed in zero wait states without the need for external cache or interleaving. When a read request misses the EDRAM's on-chip SRAM cache, the EDRAM can load a new page into cache in just 35ns (a single wait state at 25 or 33MHz bus rates). Burst write cycles are performed in only one wait state. This high level of performance is achieved with a single non-interleaved memory bank consisting of as few as eight 1M x 4 components or a single 72-pin 4Mbyte EDRAM SIMM module. Standard DRAM requires the insertion of numerous wait states due to its three times slower page cycle time and two times slower random access cycle time. The EDRAM even has fewer wait states than a much more complex writeback secondary cache plus DRAM memory subsystem as shown in figure 1.

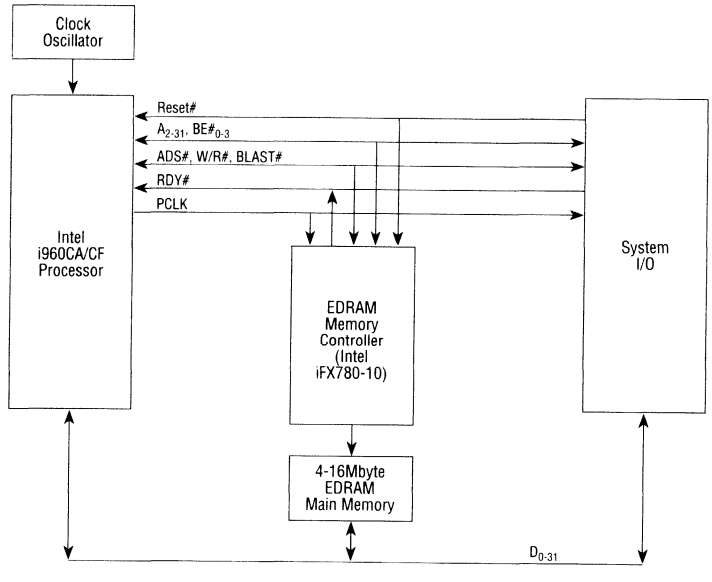
Figure 1. Bus Cycle Comparison at 33MHz Bus Speed

Transaction	EDRAM	DRAM	Cache + DRAM
Burst Read Hit	2:1:1:1	5:2:2:2	2:1:1:1
Burst Read Miss	3:1:1:1	5:2:2:2	5:2:2:2
Burst Write Hit	3:1:1:1	4:2:2:2	2:1:1:1
Burst Write Miss	3:1:1:1	4:2:2:2	4:2:2:2

A single 132-pin Intel iFX780-10 FPGA can interface 4-16Mbytes of Ramtron EDRAM main memory to a i960CA/CF processor as shown in figure 2. This design will support either 25 or 33MHz processor clock rates by simply selecting the processor clock rate and plugging in the correct speed EDRAM SIMM modules (15ns or 20ns version). This application note will describe the design of this 25 or 33MHz single chip EDRAM controller.

2

Figure 2. Intel i960CA/CF System Block Diagram



 1850 Ramtron Drive, Colorado Springs, CO 80921
Telephone (800) 545-DRAM, (719) 481-7000; Fax (719) 488-9095

EDRAM Controller Design

The objective of this single chip controller design is to support all i960CA/CF memory transactions with minimum memory wait states using a simple single phase clock design. The controller is designed to support up to four 4Mbyte EDRAM SIMM modules (DM1M32) or two 8Mbyte EDRAM SIMM modules (DM2M32) without external buffer components.

The i960 supports the following memory transactions:

- One to Four 32-bit Long Word Reads
- One to Four Byte/Word/Long Word Writes

In order to support these bus operations, the EDRAM controller must interface with the following processor control and address signals:

- A_{2-31} — Address Bus
- $BE\#_{0-3}$ — Byte Enables
- ADS# — Address Strobe Signal
- W/R# — Write/Read Mode Signal
- BLAST# — Burst Last Signal
- RDY# — Non-burst Ready Acknowledge Signal
- Reset# — Processor Reset Input
- PCLK — Processor Clock Output

The controller generates the following signals to control the EDRAM SIMM modules:

- MAL_{0-9} — Multiplex Address, Bank 0-1
- MAH_{0-9} — Multiplex Address, Bank 2-3
- $MALA_{10}$ — Bank 0, MA_{10}
- $MALB_{10}$ — Bank 1, MA_{10}
- $MAHA_{10}$ — Bank 2, MA_{10}
- $MAHB_{10}$ — Bank 3, MA_{10}
- $/RE_{0-3}$ — Row Enables for Bank 0-3
- $/CAL_{0-3}$ — Column Address Latch Inputs for Bytes 0-3
- W/R_{0-1} — Write/Read Mode Input for Low/High Banks
- $/F_{0-1}$ — Refresh Mode Input for Low/High Banks
- $/S_{0-3}$ — Chip Selects for Bank 0-3
- $/G_{0-1}$ — Output Enable for Low/High Banks
- $/WE_{0-1}$ — Write Enable for Low/High Banks

EDRAM Controller Functional Description

This section describes the EDRAM controller internal block diagram shown in figure 3.

The ***Refresh Counter*** divides the PCLK signal to generate a 62µsec refresh clock for the EDRAM. The refresh request will trigger an /F refresh on the next available bus cycle.

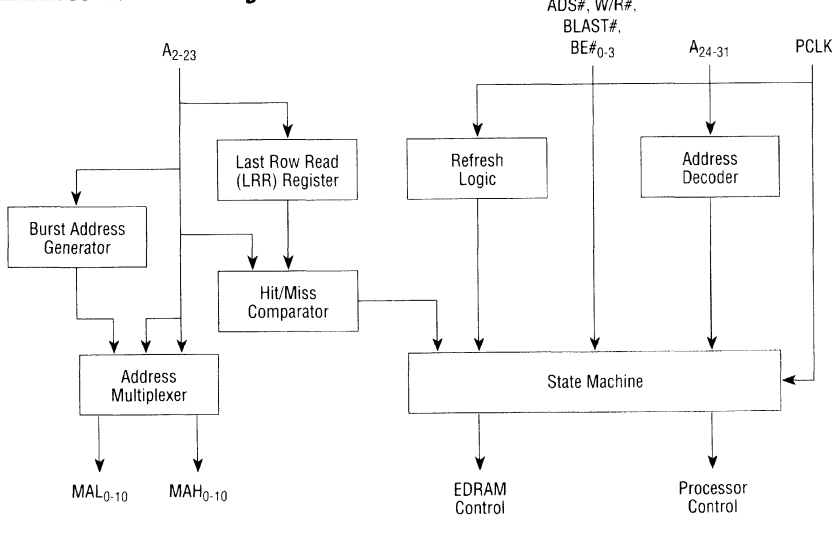
The ***Last Row Read (LRR) Register*** is a 13-bit register which holds the 11-bit row address and 2-bit bank address of the last EDRAM read event.

The ***Hit/Miss Comparator*** compares the new row and bank address with the LRR register on each read transaction. The state machine uses the hit/miss status to determine the EDRAM control sequence.

The ***Address Multiplexer*** selects either the row address, column address, or burst address to the EDRAM multiplex address inputs under the control of the state machine. Note that two independent multiplex address output busses are used for MA_{0-9} to limit the capacitance driven by the FPGA. In the case of MA_{10}, individual output pins are used for each bank of memory due to the high input capacitance of this address line. The use of multiple outputs limits the clock to output delay to 8ns to achieve the goal of zero-wait-state operation.

The ***Burst Address Generator*** increments the lower two multiplexed address bits (MA_{0-1}) using the Intel interleave sequence used during i960 cache fill and writeback cycles. The

Figure 3. EDRAM Controller Block Diagram



upper bits (MA_{2-8}) are identical to the column address.

The ***Address Decoder*** decodes the address bits (A_{24-31}) to determine if a valid memory address is present. The EDRAM memory is enabled for memory transactions in the lower 16Mbyte address range in this example. I/O and other memory devices are presumed to be mapped into the remain address space.

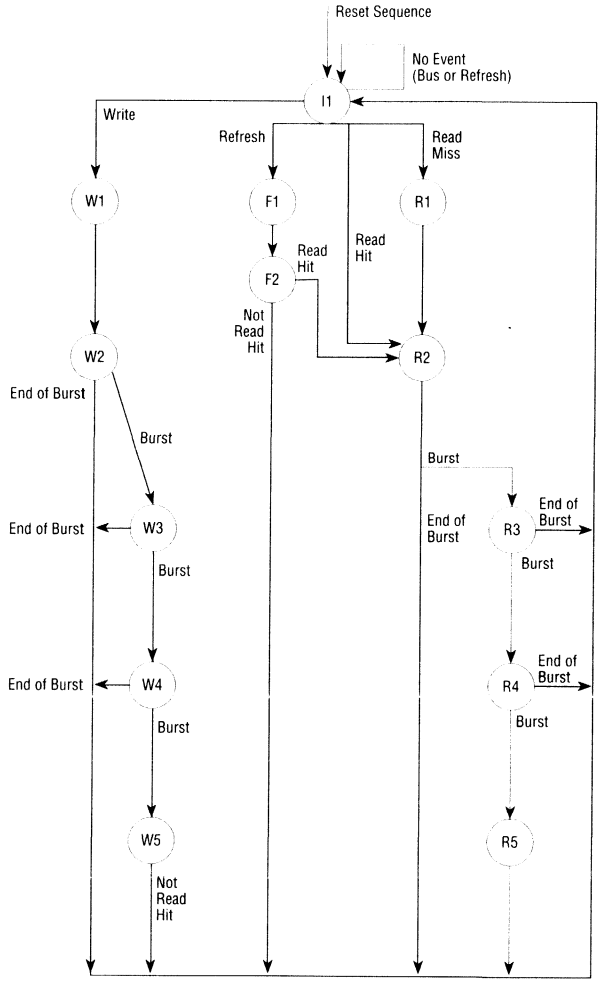
The ***State Machine*** implements the EDRAM control sequences. During reset the following sequence is run:

- *Reset Sequence* — When the Reset# input is low, the processor is in its reset state. The EDRAM controller initializes the controller logic and then enables refresh cycles. The controller will perform the required eight /F refresh cycles while Reset# is low. The required two read miss cycles per bank EDRAM initialization should be implemented in the software startup routine in the system bootstrap ROM. When Reset# is released, the controller enters its idle state waiting for memory transactions.

The detailed state diagram for the EDRAM memory sequences is shown in figure 4. A memory sequence is initiated when ADS# and a valid address are present or refresh request is pending. The W/R# input and hit/miss comparator status determine the final sequence for bus events:

- *Read Hit Sequence* — When a read hit is detected, the state machine will perform a single 32-bit read from the EDRAM cache. The read is executed by applying the column address (MAL_{0-8}, MAH_{0-8}), output enable ($/G_{0-1}$), chip select ($/S_{0-3}$) to the EDRAM, and RDY# acknowledge to the processor during R2. All control signals are available t_{CO1s} after the rising edge of the processor clock.
- *Burst Read Hit Sequence* — If the BLAST# is still high at the end of the first word transfer, the machine will continue from state R2 to the burst read sequence R3 through R5. During each state, a new burst address is output to the EDRAM at t_{CO1s}. Output enable, chip select, and the RDY# acknowledge remain valid. The burst sequence is terminated on the first cycle where BLAST# is low.
- *Read Miss Sequence* — When a read miss is detected, the state machine will perform an /RE active 32-bit read from the EDRAM. During R1, the row address (MAL_{0-10}, MAH_{0-10}), read mode (W/R low), and chip select ($/S_{0-3}$) are presented to the EDRAM. The /RE signal for the selected EDRAM bank is clocked t_{CO1a} after R1 to initiate a DRAM row access. This access will transfer the new row to SRAM cache. During R2, the column address and output enable read the cache location, and RDY# acknowledges the transfer.

Figure 4. i960CA/CF State Machine



- *Burst Read Miss Sequence* — If the BLAST# is still high at the end of the first word transfer, the machine will continue from state R2 to the burst read sequence R3 through R5. During each state a new burst address is output to the EDRAM at t_{CO1s}. Output enable, chip select, and RDY# acknowledge remain valid. The burst sequence is terminated on the first cycle where BLAST# is low.
- *Write Sequence* — An /RE active single write cycle is performed. The bytes written are determined by the $BE\#_{0-3}$ input. The state machine activates the appropriate $/CAL_{0-3}$ outputs to enable the correct bytes of memory. The state machine selects the row address (MAL_{0-10}, MAH_{0-10}), write mode (W/R high), and appropriate chip select ($/S_{0-3}$) signals to

the EDRAM during W1. /RE is enabled t_{CO1a} after the beginning of W1. The column address is output at t_{CO1s} of W2. The /WE and /CAL outputs for the selected bytes are enabled at t_{CO1a} after the middle of W2 to initiate the write cycle. /WE, /CAL, and /RE are brought high to terminate the write.

- *Burst Write Sequence* — If BLAST# is high during W1, the processor will continue to output burst data. In this case, the controller will proceed to W3 through W5 until BLAST# becomes low. On each cycle, a new column address is generated using the Intel interleave format and the /WE and /CAL are brought low to write data. The write is terminated in the last write state by bringing /CAL, /WE, and /RE high.
- *Refresh* — If a refresh is pending during I1, the state machine will perform an internal refresh on the next cycle by jumping to F1. Refresh mode (/F) is enabled during F1. /RE is enabled t_{CO1a} after F1 to perform the internal refresh cycle. The next bus event is pipelined during F2. If the next event is a read hit, the state machine jumps directly to R2 to perform the cache read while the DRAM precharge time is met. If the next event requires another DRAM cycle, the state machine jumps to I1 to allow a single wait state while the precharge time is met.

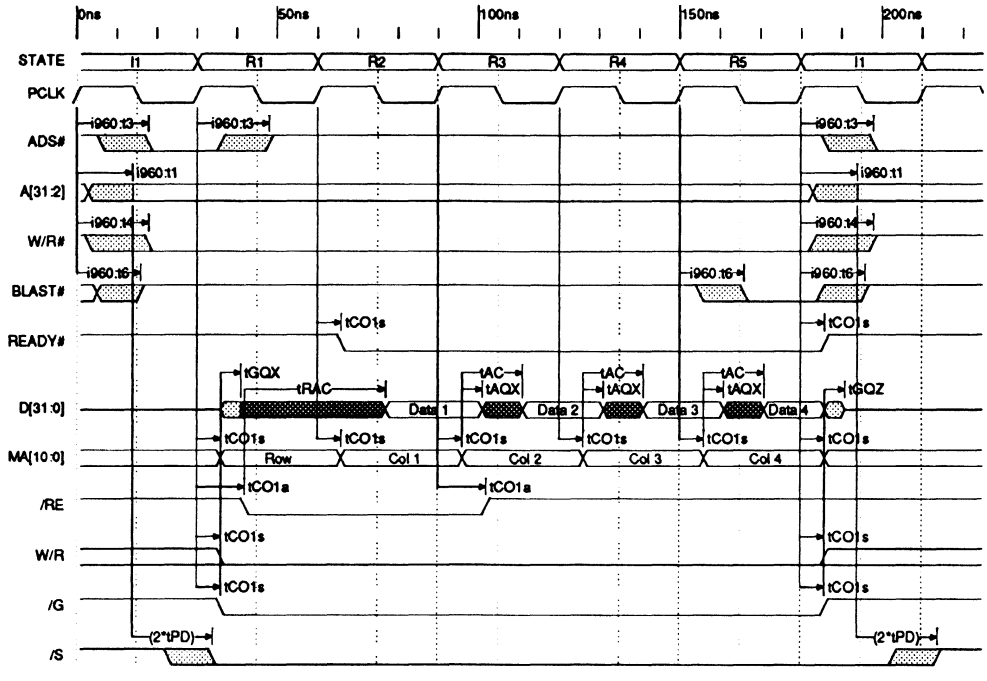
Note that the EDRAM control interface is partitioned to make sure that the output capacitance does not cause the clock to output time on any signal to exceeded 8ns. As a result, heavily loaded signals such as W/R, /F, /WE, /G are split into two pins which drive either the low or high two banks of memory. On the other hand, the $/CAL_{0-3}$ signals are lightly loaded and a single pin drives all four banks of memory.

The attached burst read miss, burst read hit, and burst write timing sequences demonstrate the timing of the EDRAM controller in a 33MHz i960CA/CF system with the 15ns version of the EDRAM. The same design will work at 25MHz using the lower cost 20ns version of the EDRAM. The worst case timing analysis is performed using Chronology's Timing Designer™ software with EDRAM timing parameters entered from the databook. EDRAM controller parameters are from the Intel 132-pin iFX780-10 FPGA datasheet with derating for additional load capacitance. The Intel FPGA was selected because of its fast clock to output delay (6ns into 30pf), fast setup time (6.5ns), and its fast address comparator feature which allows implementation of a single chip EDRAM controller. Other FPGA or PAL devices with similar performance should also be useful to perform an EDRAM controller design. In high volume applications, this controller design should be convertible into a low cost CMOS gate array device with recurring cost of less than five dollars.

Conclusion

A single chip EDRAM controller for the 25 and 33MHz Intel i960CA/CF microprocessor can be implemented using a high performance FPGA such as the Intel iFX780. This controller supports up to 16Mbytes of EDRAM without additional buffer components. Ramtron's EDRAM improves i960CA/CF system performance by significantly reducing the number of wait states over a standard DRAM or secondary SRAM cache plus DRAM. This system should provide one of the fastest and most integrated embedded control solutions available.

Word Burst Read Miss



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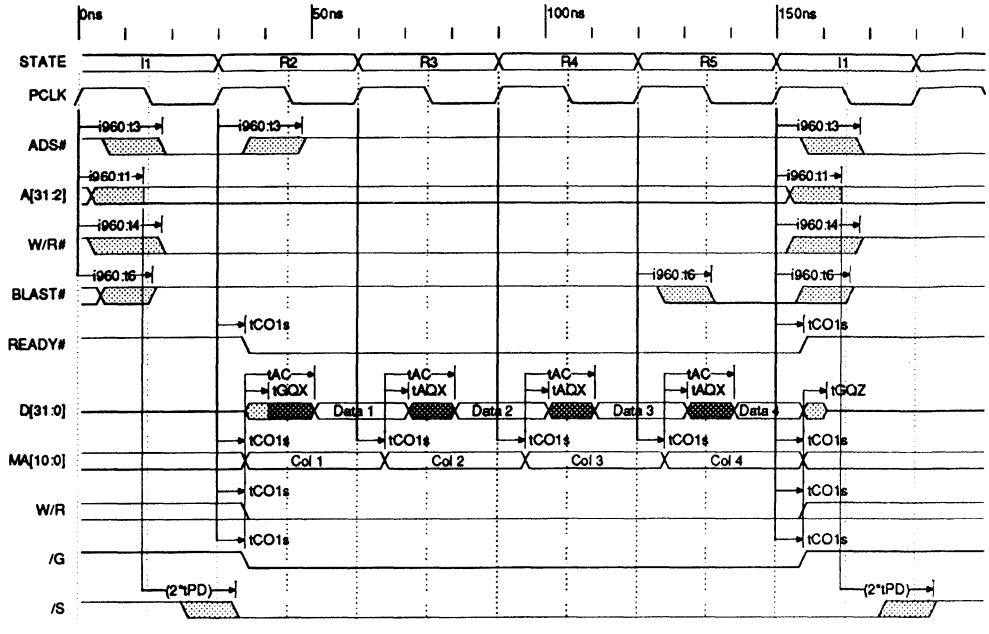
Parameter Table

Name	Min	Max	Comment
i960:t1	3	14	PCLK to A(31:2) to Output Valid Delay
i960:t3	6	18	PCLK to ADS# Output Valid Delay
i960:t4	3	18	PCLK to W/R# Output Valid Delay
i960:t6	5	16	PCLK to BLAST# and WAIT# Output Valid Delay
i960:t11	3	16	PCLK to D(31:0) Output Valid Delay
i960:tOF	3	22	PCLK to ALL SIGNALS Output Float Delay
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1d		8	CLK to Output Valid (Delayed)
tCO1a		12	CLK to Output Valid (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn Off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

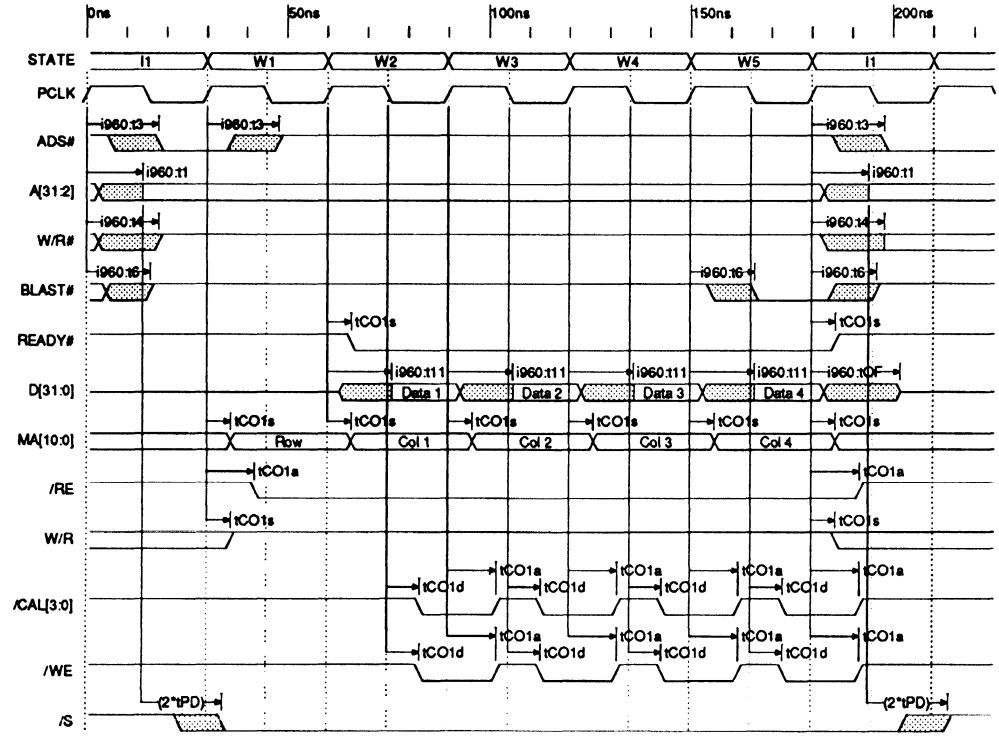
Word Burst Read Hit



Parameter Table

Name	Min	Max	Comment
i960:t1	3	14	PCLK to A(31:2) to Output Valid Delay
i960:t3	6	18	PCLK to ADS# Output Valid Delay
i960:t4	3	18	PCLK to W/R# Output Valid Delay
i960:t6	5	16	PCLK to BLAST# and WAIT# Output Valid Delay
i960:t11	3	16	PCLK to D(31:0) Output Valid Delay
i960:tOF	3	22	PCLK to ALL SIGNALS Output Float Delay
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1d		8	CLK to Output Valid (Delayed)
tCO1a		12	CLK to Output Valid (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn Off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

Word Burst Write



Parameter Table

Name	Min	Max	Comment
i960:t1	3	14	PCLK to A(31:2) to Output Valid Delay
i960:t3	6	18	PCLK to ADS# Output Valid Delay
i960:t4	3	18	PCLK to W/R# Output Valid Delay
i960:t6	5	16	PCLK to BLAST# and WAIT# Output Valid Delay
i960:t11	3	16	PCLK to D(31:0) Output Valid Delay
i960:tOF	3	22	PCLK to ALL SIGNALS Output Float Delay
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1d		8	CLK to Output Valid (Delayed)
tCO1a		12	CLK to Output Valid (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn Off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

EDRAM Controller For Intel 486DX2 50MHz & 66MHz Microprocessors

Application Note

Summary

Ramtron's EDRAM is the ideal memory for high performance PC systems.

- No Wait States During Burst Read Hit and Write Cycles
- Only One Wait State During a Burst Read Miss Cycle
- Single Chip FPGA-based Controller Solution

Introduction

The Intel 486DX2 microprocessor is the most popular microprocessor for high performance personal computer applications. The 486DX2 has 32-bit integer and floating point units, a paged virtual memory management unit (MMU), and an 8Kbyte cache for instructions and data. The 486DX2 operates the external bus at a 1X clock rate and clock doubles the on-chip clock to operate the CPU at a 2X clock rate. 486DX2 processors are available in 50 or 66MHz versions. The external bus interface has separate 32-bit address and data busses and supports synchronous one to four word burst read transfers and single word write transfers. Ready and burst ready signals allow the external memory controller to insert wait states as necessary to meet the memory subsystems timing requirements.

Ramtron's enhanced DRAM (EDRAM) memory is the ideal main memory component to support the 486DX2 processors. Its fast 15ns read access time allows all read cycles which hit the on-chip cache to be performed in zero wait states without an external cache or interleaving. When a read request misses the EDRAM's on-chip SRAM cache, the EDRAM can load a new page into cache in just 35ns (a single wait state at 25 or 33MHz bus rates). Write cycles are posted in zero wait states. This high level of performance is achieved with a single non-interleaved memory consisting of as few as eight 1M x 4 components or a single 72-pin 4Mbyte EDRAM SIMM module. Standard DRAM requires the insertion of numerous wait states due to its three times slower page cycle time and two times slower random access cycle time. The EDRAM even has fewer wait states than a much more complex secondary cache plus DRAM memory subsystem as shown in figure 1.

Figure 1. Bus Cycle Comparison at 33MHz Bus Speed

Transaction	EDRAM	DRAM	Cache + DRAM
Burst Read Hit	2:1:1:1	5:2:2:2	2:1:1:1
Burst Read Miss	3:1:1:1	5:2:2:2	5:2:2:2
Write Hit	2	4	2
Write Miss	2	4	4

Four to sixteen megabytes of Ramtron EDRAM main memory can be interfaced to a 486DX2 microprocessor and standard ISA/VL bus adapter chip such as the Opti 495SLC using a single high performance FPGA chip (such as the Intel iFX780 shown in figure 2)

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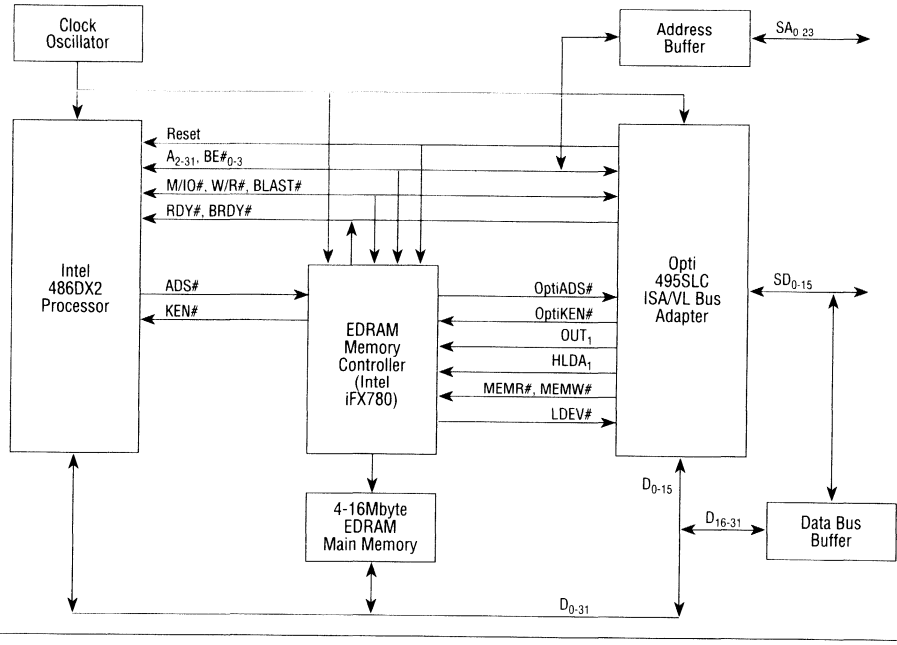
Figure 2. 486DX2-66 System Block Diagram



Such a design will support both 50 and 66MHz processor clock rates using a common motherboard design by simply inserting the appropriate processor and EDRAM SIMM modules. This application note will describe the design of a 50 or 66MHz 486DX2 single chip EDRAM controller. A future application note will discuss a two-way interleave controller design for the 40 and 50MHz 486DX processors from Intel, AMD, and Cyrix.

EDRAM Controller Design

The objective of this single chip controller design is to support all 486DX2 memory transactions with minimum memory wait states using a simple single phase clock design. The controller is designed to support up to four 4Mbyte EDRAM SIMM modules (DM1M32) or two 8Mbyte EDRAM SIMM modules (DM2M32) without external buffer components. The controller is also designed to support ISA bus master, DMA, and VL bus master cycles.

The 486 supports the following memory transactions:

- One to Four 32-bit Long Word Reads
- Single Byte/Word/Long Word Write

In order to support these bus operations, the EDRAM controller must interface with the following processor control and address signals:

- A_{2-31} — Address Bus
- $BE\#_{0-3}$ — Byte Enables
- M/IO# — Memory/I/O Mode Signal
- W/R# — Write/Read Mode Signal
- ADS# — Address Strobe Signal
- BLAST# — Burst Last Signal
- RDY# — Non-burst Ready Acknowledge Signal
- BRDY# — Burst Ready Acknowledge Signal
- KEN# — Cache Enable Signal

The controller must interface with the following Opti 495SLC chip signals:

- OptiADS# — Opti Address Strobe Input
- OptiKEN# — Opti Cache Enable Output
- Reset# — Opti Reset Output
- LDEV# — Opti VL Bus Local Device Input
- $HLDA_1$ — Opti Hold Acknowledge Output
- MEMR# — ISA Bus Memory Read Signal
- MEMW# — ISA Bus Memory Read Signal
- OUT1 — Opti Refresh Clock

The controller generates the following signals to the EDRAM SIMM modules:

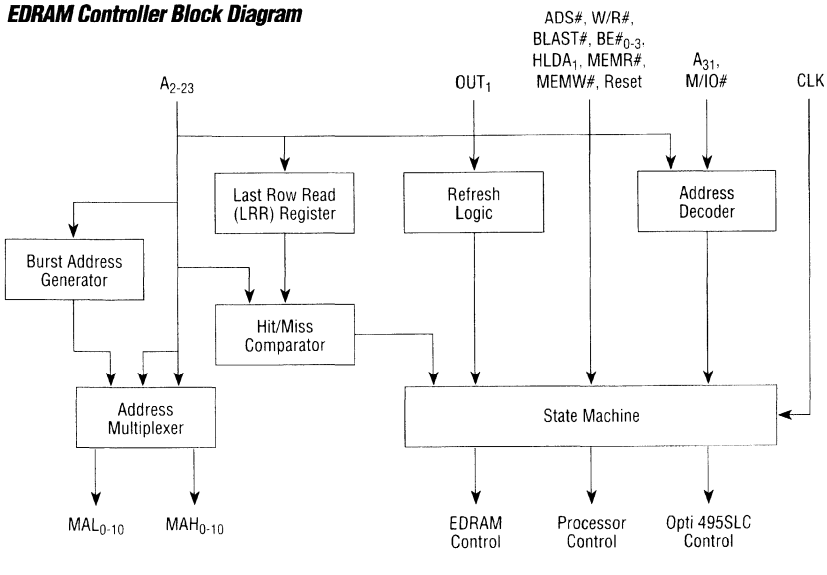
- MAL_{0-9} — Multiplex Address, Bank 0-1
- MAH_{0-9} — Multiplex Address, Bank 2-3
- $MALA_{10}$ — Bank 0, MA_{10}
- $MALB_{10}$ — Bank 1, MA_{10}
- $MAHA_{10}$ — Bank 2, MA_{10}
- $MAHB_{10}$ — Bank 3, MA_{10}
- $/RE_{0-3}$ — Row Enables for Bank 0-3
- $/CAL_{0-3}$ — Column Address Latch Inputs for Bytes 0-3
- W/R_{0-1} — Write/Read Mode Input for Low/High Banks
- $/F_{0-1}$ — Refresh Mode Input for Low/High Banks
- $/S_{0-3}$ — Chip Selects for Bank 0-3
- $/G_{0-1}$ — Output Enable for Low/High Banks
- $/WE_{0-1}$ — Write Enable for Low/High Banks

EDRAM Controller Functional Description

This section describes the EDRAM controller internal block diagram shown in figure 3.

The ***Refresh Logic*** receives the OUT_1 signal from the ISA logic. This signal is a 15µsec refresh clock generated by the

Figure 3. EDRAM Controller Block Diagram



82C206 timer. On the rising edge of the 15µsec clock, a refresh request is generated to the state machine. This signal will trigger an immediate refresh on the next available bus cycle.

The ***Last Row Read (LRR) Register*** is a 13-bit register which holds the 11-bit row address and 2-bit bank address of the last EDRAM read event.

The ***Hit/Miss Comparator*** compares the new row and bank address with the LRR register on each read event. The state machine uses the hit/miss status to determine the EDRAM control sequence.

The ***Address Multiplexer*** selects either the row address, column address, or burst address to the EDRAM multiplex address inputs under the control of the state machine. Note that two independent multiplex address output busses are used for MA_{0-9} to limit the capacitance driven by the FPGA. In the case of MA_{10}, individual output pins are used for each bank of memory due to the high input capacitance of this address line. The use of multiple outputs limits the clock to output delay to 8ns to achieve the system performance goal.

The ***Burst Address Generator*** increments the lower two multiplexed address bits (MA_{0-1}) using the Intel interleave sequence used during 486 cache fill cycles. The upper bits (MA_{2-8}) are identical to the column address.

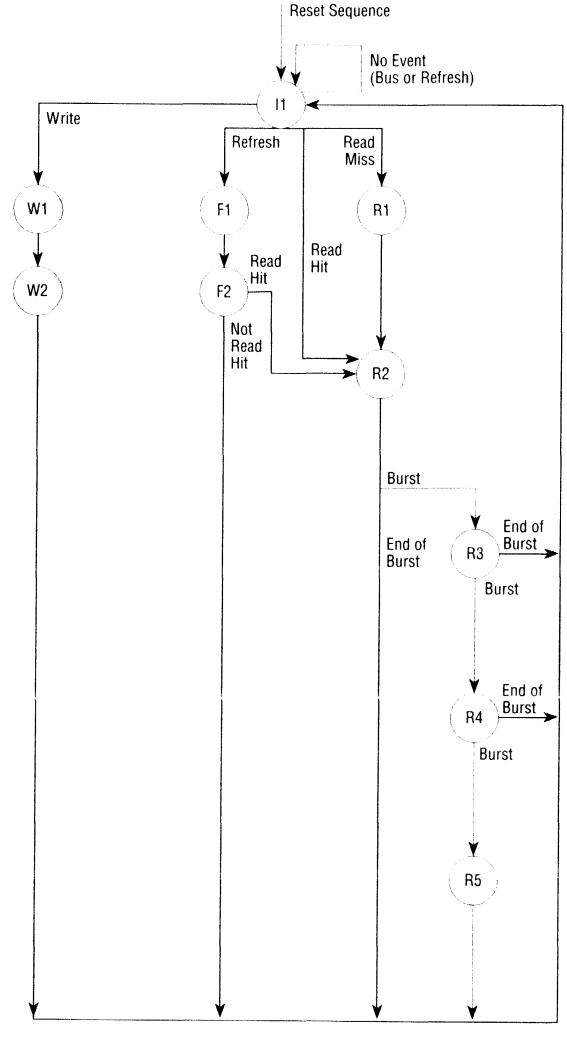
The ***Address Decoder*** decodes the address bits (A_{2-23}, A_{31}) and the M/IO# mode bit to determine if a valid memory address is present. The EDRAM memory is enabled for memory transactions in the lower 16Mbyte address range with the exception of the high memory region (640K-1M).

The ***State Machine*** implements the EDRAM control sequences. During reset the following sequence is run:

- *Reset Sequence* — When the Reset input is high, the processor is in its reset state. The EDRAM controller initializes the controller logic and then enables refresh cycles. Processor or DMA cycles are disabled while Reset is high. The controller will perform the required eight /F refresh cycles while Reset is high. The required two read miss cycles per bank EDRAM initialization should be implemented in the software startup routine in the BIOS ROM. When Reset is released, the controller enters its idle state waiting for memory events.

The detailed state diagram for the EDRAM memory sequences is shown in figure 4. A memory sequence is initiated when ADS# and a valid address are present (processor or VL bus master cycles), $HLDA_I$ and a valid address are present (ISA master or DMA cycles), or an urgent refresh request is pending. The W/R#, MEMR#, MEMW#, and hit/miss comparator status determine the final sequence for bus events:

Figure 4. 486DX2 State Machine



- *Read Hit Sequence* — When a read hit is detected, the state machine will perform a single 32-bit read from the EDRAM cache. The read is executed by applying the column address (MAL_{0-8}, MAH_{0-8}), output enable ($/G_{0-1}$), and the appropriate chip select ($/S_{0-3}$) to the EDRAM, and the BRDY# acknowledge to the processor during R2. All control signals are available t_{CO1s} after the rising edge of the processor clock. The 495SLC is inhibited by driving LDEV# and disabling OptiADS# during EDRAM cycles.

- *Burst Read Hit Sequence* — If the BLAST# is still high at the end of the first word transfer, the machine will continue from state R2 to the burst read sequence R3 through R5. During each state a new burst address is output to the EDRAM at t_{CO1s} after the clock. Output enable, chip select, and the BRDY# acknowledge remain valid. The burst sequence is terminated on the first cycle where BLAST# is low.
- *Read Miss Sequence* — When a read miss is detected, the state machine will perform an /RE active 32-bit read from the EDRAM. During R1, the row address (MAL_{0-10}, MAH_{0-10}), read mode (W/R low), and chip select ($/S_{0-3}$) are presented to the EDRAM. The /RE signal for the selected EDRAM bank is clocked t_{CO1a} after R1 to initiate a DRAM row access. This access will transfer the new row to SRAM cache. During R2, the column address and output enable are output to read the cache location, and the BRDY# acknowledge is generated to the processor to acknowledge the access. The 495SLC is inhibited by driving LDEV# and disabling OptiADS# during EDRAM cycles.
- *Burst Read Miss Sequence* — If the BLAST# is still high at the end of the first word transfer, the machine will continue from state R2 to the burst read sequence R3 through R5. During each state a new burst address is output to the EDRAM at t_{CO1s} after the clock. Output enable, chip select, and the BRDY# acknowledge remain valid. The burst sequence is terminated on the first cycle where BLAST# is low.
- *Write Sequence* — An /RE active single write cycle is performed. The bytes written are determined by the $BE\#_{0-3}$ input. The state machine activates the appropriate $/CAL_{0-3}$ outputs to enable the correct bytes of memory. The state machine selects the row address (MAL_{0-10}, MAH_{0-10}), write mode (W/R high), and appropriate chip select ($/S_{0-3}$) signals to the EDRAM, and the RDY# acknowledges to the processor during W1. /RE is enabled t_{CO1a} after the beginning of W1. The column address is output and /WE is enabled to latch data during W2. The /CAL outputs for the selected bytes are enabled at t_{CO2s} after W2 to initiate the write cycle. The write is terminated at the end of W2 by bringing /CAL, /WE, and /RE high.
- *Refresh* — If a refresh is pending during I1, the state machine will perform an internal refresh on the next cycle by jumping to F1. Refresh mode (/F) is enabled during F1. /RE is enabled t_{CO1a} after F1 to perform the refresh cycle. The next bus event is pipelined during F2. If the next event is a read hit, the state machine jumps directly to R2 to perform the cache read while the DRAM precharge time is met. If the next event requires another DRAM cycle, the state machine jumps to I1 to allow a single wait state while the precharge time is met.

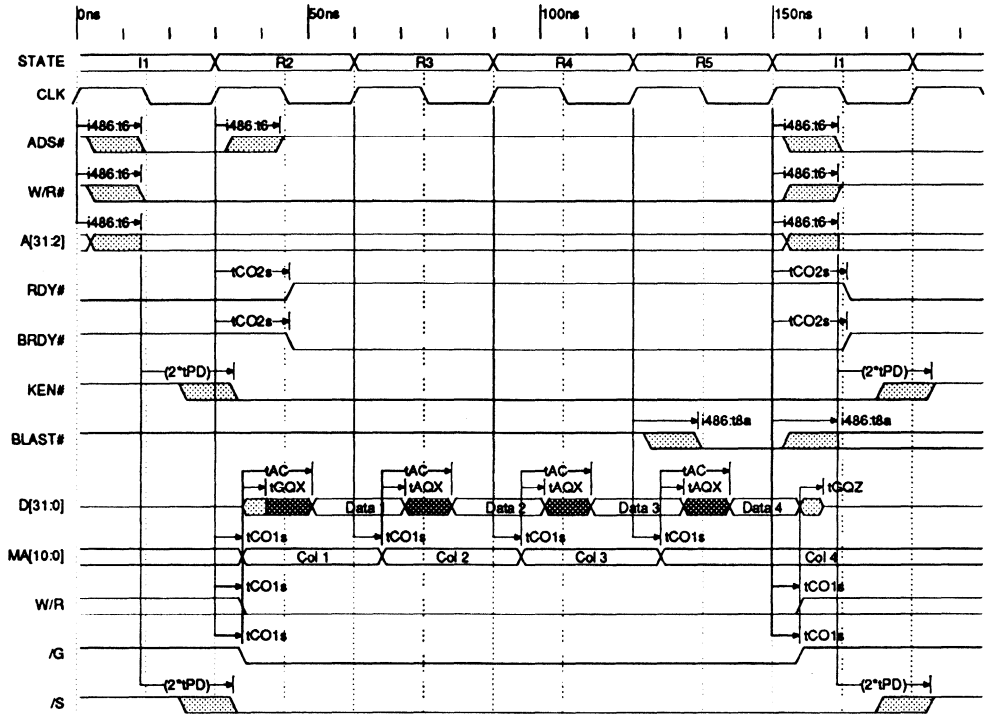
Note that the EDRAM control interface is partitioned to make sure that the output capacitance does not cause the clock to output time on any signal to exceeded 8ns. As a result, heavily loaded signals such a W/R, /F, /WE, /G are split into two pins which drive either the low or high two banks of memory. On the other hand, the $/CAL_{0-3}$ signals are lightly loaded and a single pin drives all four banks of memory.

The attached burst read hit, burst read miss, and write timing sequences demonstrate the timing of the EDRAM controller in a 66MHz 486DX2 system environment with the 15ns version of the EDRAM. The same design will work at 50MHz using the lower cost 20ns version of the EDRAM. The worst case timing analysis is performed using Chronology's Timing Designer™ software with EDRAM timing parameters entered from the databook. EDRAM controller parameters are from the Intel 132-pin iFX780 FPGA datasheet. The Intel FPGA was selected because of its fast clock to output delay (6ns into 30 pf), fast setup time (6.5ns), and its fast address comparator feature which match EDRAM control requirements. Other FPGA or PAL devices with similar performance should also be useful to perform an EDRAM controller design. In high volume applications, this controller design should be convertible into a low cost CMOS gate array device with recurring cost of less than five dollars.

Conclusion

A single chip EDRAM controller can be implemented using a high performance FPGA such as the Intel iFX780. This controller supports up to 16Mbytes of EDRAM without additional buffer components. Ramtron's EDRAM improves 486DX2 system performance by significantly reducing the number of wait states over a standard DRAM or secondary SRAM cache plus DRAM.

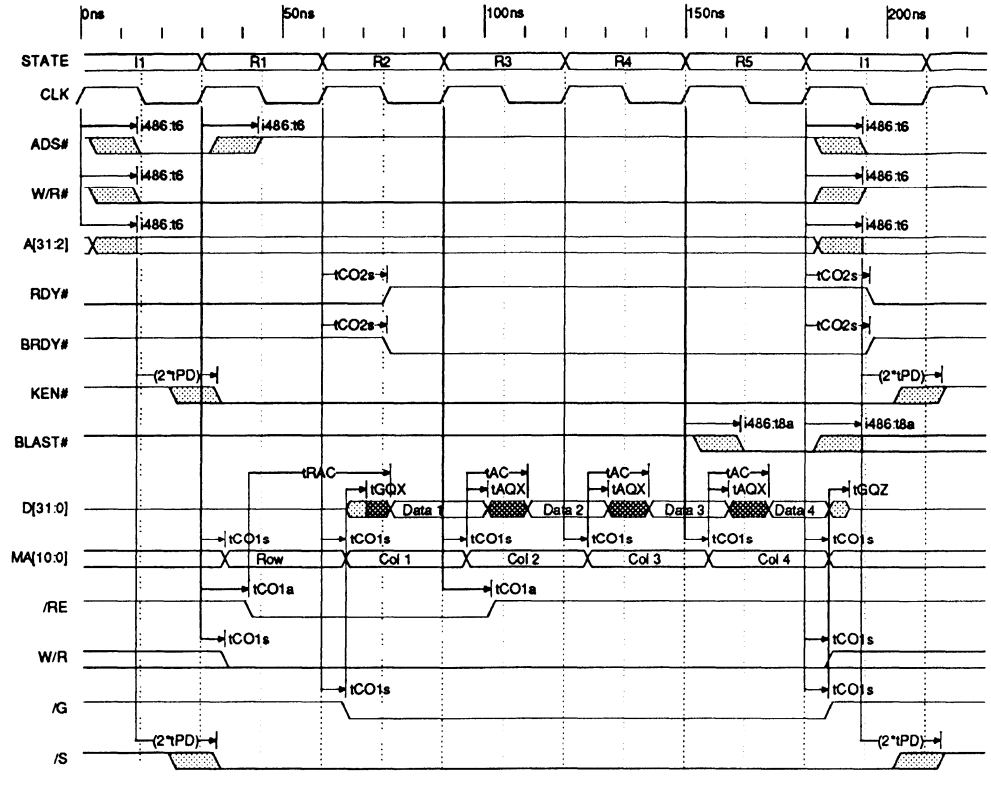
Four Word Burst Read Hit Timing



Parameter Table

Name	Min	Max	Comment
i486.t6	3	14	A(31:2), PWT, PCD, BE#(3:0), M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BRGE#, HLDA Valid Delay
i486:t8a	3	14	BLAST#, PLOCK# Valid Delay
i486:t10	3	14	D(31:0), DP(3:0) Write Data Valid Delay
i486:t11		20	D(31:0), DP(3:0) Write Data Float Delay
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1a		12	CLK to Output Valid (Asynchronous)
tCO2s		16	CLK to Output Valid Fed Through Combinational Macrocell (Synchronous)
tCO2a		22	CLK to Output Valid Fed Through Combinational Macrocell (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tAQX	5		Column Address Valid to Output Turn On
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn Off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

Four Word Burst Read Miss Timing



Parameter Table

Name	Min	Max	Comment
i486.t6	3	14	A(31:2), PWT, PCD, BE#(3:0), M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BRGE#, HLDA Valid Delay
i486:t8a	3	14	BLAST#, PLOCK# Valid Delay
i486:t10	3	14	D(31:0), DP(3:0) Write Data Valid Delay
i486:t11		20	D(31:0), DP(3:0) Write Data Float Delay
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1a		12	CLK to Output Valid (Asynchronous)
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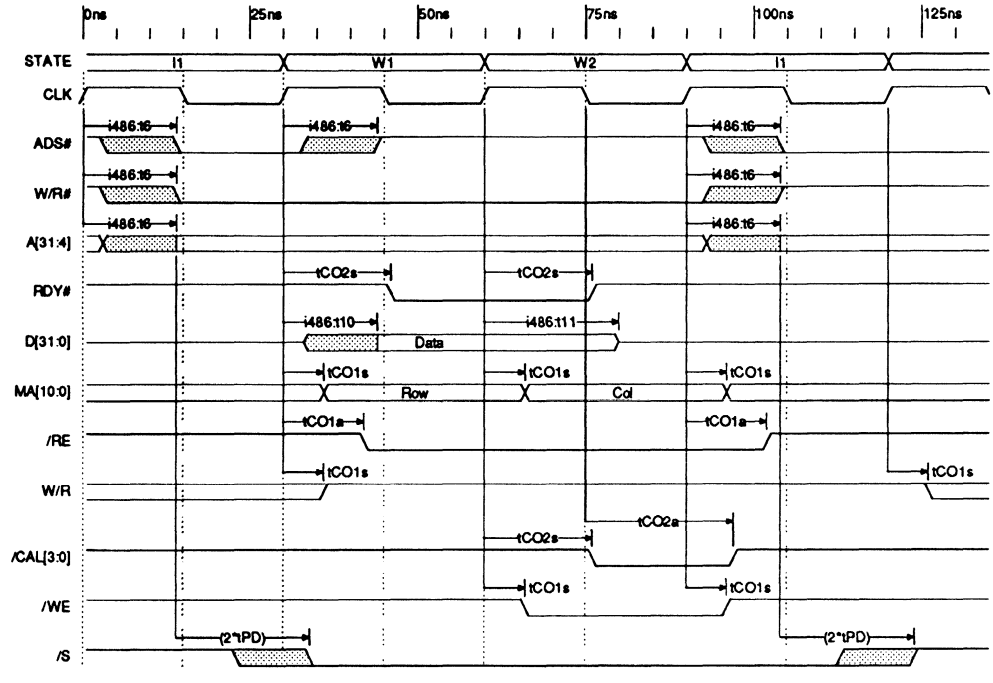
tCO2a		22	CLK to Output Valid Fed Through Combinational Macrocell (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tAQX	5		Column Address Valid to Output Turn On
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn Off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

One Word Write Timing



Parameter Table

Name	Min	Max	Comment
i486:t6	3	14	A(31:2), PWT, PCD, BE#(3:0), M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BRGE#, HLDA Valid Delay
i486:t8a	3	14	BLAST#, PLOCK# Valid Delay
i486:t10	3	14	D(31:0), DP(3:0) Write Data Valid Delay
i486:t11		20	D(31:0), DP(3:0) Write Data Float Delay
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1a		12	CLK to Output Valid (Asynchronous)
tCO2s		16	CLK to Output Valid Fed Through Combinational Macrocell (Synchronous)
tCO2a		22	CLK to Output Valid Fed Through Combinational Macrocell (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tAQX	5		Column Address Valid to Output Turn On
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn Off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

EDRAM Controller For Motorola 68040 25MHz & 33MHz Microprocessors

Application Note

Summary

Ramtron's EDRAM is the ideal memory for high performance 68040 systems.

- No Wait States During Burst Read Hit and Write Cycles
- Only One Wait State During Burst Read Miss Cycles
- Single Chip FPGA-based Controller Solution

Introduction

The Motorola 68040 is one of the most popular microprocessors for embedded control and computer applications. The 68040 has 32-bit integer (IU) and floating point (FPU) units, instruction and data memory management units (MMU), and 4Kbyte instruction and data caches. The CPU operates from a 2X clock input (PCLK), and the external bus operates from a 1X clock (BCLK). The 68040 is available in 25, 33, and 40MHz versions. Its external bus interface has separate 32-bit address and data busses and supports synchronous single and four-word read/write transfers. A transfer acknowledge signal allows the external memory controller to insert wait states as necessary to meet the memory timing requirements.

Ramtron's enhanced DRAM (EDRAM) memory is the ideal main memory component to support the 68040 when operating at 25 or 33MHz clock rates. Its fast 15ns page read and write cycle times allow both single and four-word burst read and write transactions to be performed in zero wait states. When a read request misses the EDRAM's on-chip SRAM cache, the EDRAM can load a new page into cache in just 35ns (a single wait state at 25 or 33MHz). This high level of performance is achieved with a single non-interleaved memory consisting of as few as eight 1M x 4 components or a single 72-pin 4Mbyte EDRAM SIMM module. Standard DRAM requires the insertion of numerous wait states due to its three times slower page mode cycle time and two times slower random access cycle time. The EDRAM even has fewer wait states than a much more complex secondary cache plus DRAM memory subsystem, as shown in figure 1.

Figure 1. Bus Cycle Comparison at 33MHz Bus Speed

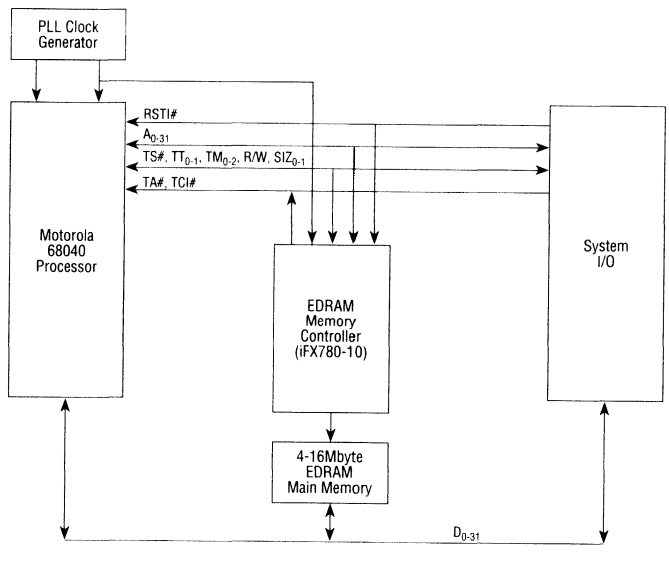
Transaction	EDRAM	DRAM	Cache + DRAM
Burst Read Hit	2:1:1:1	3:2:2:2	2:1:1:1
Burst Read Miss	3:1:1:1	7:2:2:2	3:2:2:2/7:2:2:2*
Burst Write Hit	2:1:1:1	3:2:2:2	2:1:1:1
Burst Write Miss	2:1:1:1	6:2:2:2	3:2:2:2/6:2:2:2*

*DRAM Page Hit/Miss Cycles

Ramtron's EDRAM can be interfaced to a 68040 microprocessor using a single high performance FPGA chip (such as the Intel iFX780 shown in figure 2) and a PLL clock doubler chip. This application note will describe the design of a 25 or 33MHz 68040 single chip EDRAM controller. A future application note will discuss a controller design for the 40MHz version of the 68040.

2

Figure 2. 68040 System Block Diagram



EDRAM Controller Design

The objective of this single chip controller design is to support all 68040 memory transactions with minimum memory wait states while driving either four 4Mbyte EDRAM SIMM modules (DM1M32) or two 8Mbyte EDRAM SIMM modules (DM2M32).

The 68040 supports the following memory transactions for user and supervisor data spaces:

- Single Byte/Word/Long Word Read
- Single Byte/Word/Long Word Write
- Four Long Word Burst Read
- Four Long Word Burst Write

In order to support these bus operations, the EDRAM controller must interface with the following control and address signals:

- A_{0-31} — Address Bus
- TT_{0-1} — Transfer Type
- TM_{0-2} — Transfer Mode
- SIZ_{0-1} — Transfer Size
- R/W — Read/Write
- /TS — Transfer Start
- /TA — Transfer Acknowledge
- /TCI — Transfer Cache Inhibit
- /RSTI — Reset In
- BCLK — Bus Clock (1X)

The controller generates the following signals to the EDRAM SIMM modules:

- MAL_{0-9} — Multiplexed Address, Bank 0-1
- MAH_{0-9} — Multiplexed Address, Bank 2-3
- $MALA_{10}$ — Bank 0 A10
- $MALB_{10}$ — Bank 1 A10
- $MAHA_{10}$ — Bank 2 A10
- $MAHB_{10}$ — Bank 3 A10
- $/RE_{0-3}$ — Row Enables for Bank 0-3
- $/CAL_{0-3}$ — Column Address Latch Inputs for Bytes 0-3
- W/R_{0-1} — Write/Read Mode Input for Low/High Banks
- $/F_{0-1}$ — Refresh Mode Input for Low/High Banks
- $/S_{0-3}$ — Chip Selects for Bank 0-3
- $/G_{0-1}$ — Output Enable for Low/High Banks
- $/WE_{0-1}$ — Write Enable for Low/High Banks

The EDRAM controller internal block diagram is shown in figure 3.

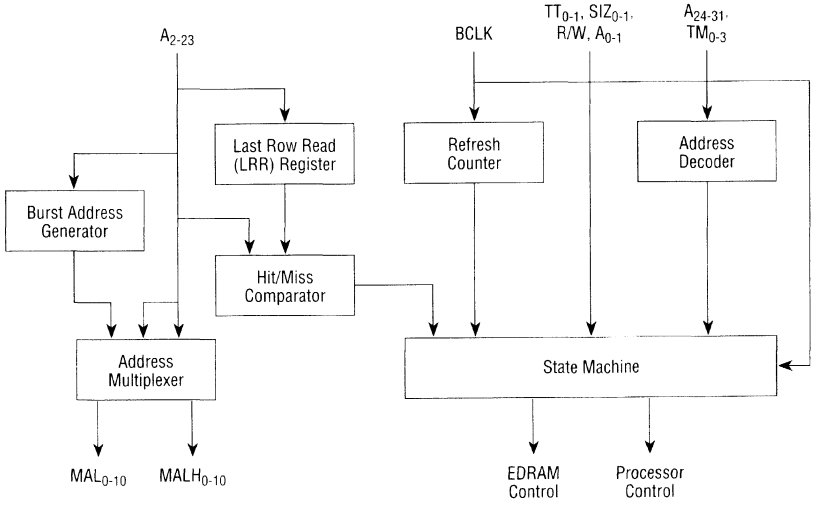
EDRAM Controller Functional Description

The ***Refresh Counter*** divides the BCLK input down to generate a 62µsec refresh clock. This signal is used to trigger refresh cycles at a rate sufficient to refresh all rows every 64ms. The refresh request will trigger a refresh cycle on the next available bus cycle.

The ***Last Row Read (LRR) Register*** is a 13-bit register which holds the 11-bit row address and 2-bit bank address of the last EDRAM read event.

The ***Hit/Miss Comparator*** compares the new row and bank address with the LRR register on each read event. The state machine uses the hit/miss status to determine the EDRAM control sequence.

Figure 3. EDRAM Controller Block Diagram



The ***Address Multiplexer*** selects either the row address, column address, or burst address to the EDRAM multiplex address inputs under the control of the state machine.

The ***Burst Address Generator*** increments the lower two multiplexed address bits (MA_{0-1}) using the mod-4 linear wrap sequence used during 68040 cache fill cycles. The upper bits (MA_{2-8}) are identical to the column address.

The ***Address Decoder*** decodes the upper address bits (A_{24-31}) and the transfer mode bits (TM_{0-2}) to determine if a valid memory address is present. EDRAM memory is enabled for the lower 16-Mbyte address range of the user and supervisor memory segments.

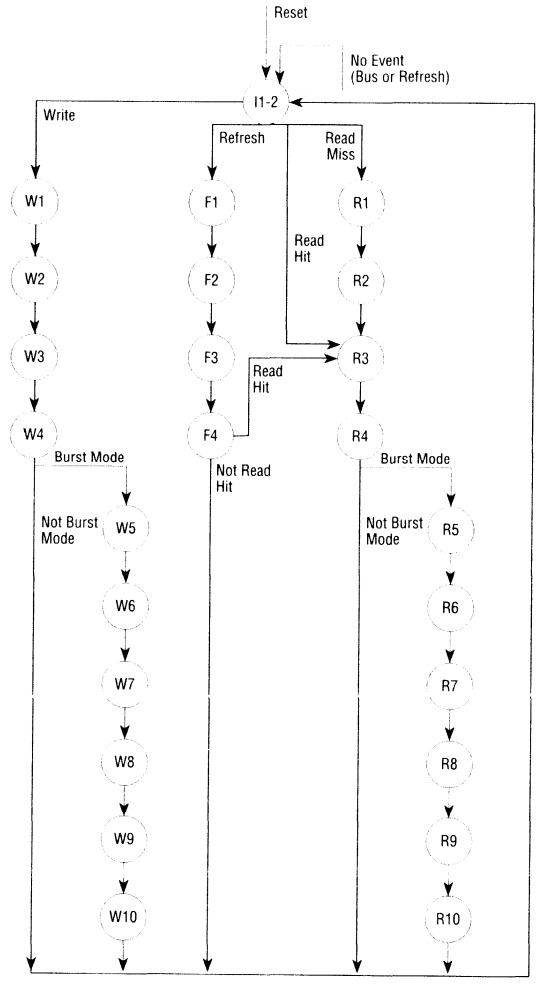
The ***State Machine*** implements the EDRAM control sequence. During reset the following sequence is run:

- *Reset Sequence* — When the /RSTI input is low, the processor is in its reset state. The EDRAM controller initializes the controller logic and then enables refresh cycles. The controller will perform at least eight /F refresh cycles while /RSTI is low to initialize the EDRAM. When /RSTI is released, the controller enters its idle state waiting for memory events. At least two read miss cycles should be performed to each bank of EDRAM by the system startup software in bootstrap ROM to complete EDRAM initialization.

The detailed state diagram for the EDRAM memory sequences is shown in figure 4. A memory sequence is initiated when a transfer strobe and valid address are present or a refresh refresh request is pending. The transfer type and hit/miss comparator status determine the final sequence for bus events:

- *Read Hit Sequence* — When a read hit is detected, the state machine will perform a single long word read from the EDRAM cache. The read is executed by applying the column address (MAL_{0-8}, MAH_{0-8}), output enable ($/G_{0-1}$), and chip select ($/S_{0-3}$) to the EDRAM and the transfer acknowledge (/TA) to the processor at t_{CO1s} of R3.
- *Burst Read Hit Sequence* — If the transfer mode specifies a four long word burst, the state machine will continue from state R4 to the burst read sequence R5 through R10. During each pair of states (i.e., R5, R6, etc.), a new burst address is output to the EDRAM at t_{CO1s}. The output enable, chip select, and transfer acknowledge remain valid.
- *Read Miss Sequence* — When a read miss is detected, the state machine will perform an /RE active long word read from the EDRAM. During R1, the row address (MAL_{0-10}, MAH_{0-10}), read mode (W/R low), and chip select ($/S_{0-3}$) are presented to the EDRAM at t_{CO1s}. The /RE signal to the selected EDRAM bank is clocked to initiate a DRAM row access at t_{CO1a}. This access will transfer the new row to SRAM cache. During R3, the column address and output enable are output to read the cache location and /TA acknowledges the access at t_{CO1s}.

Figure 4. 68040 State Machine



- *Burst Read Miss Sequence* — If the transfer mode specifies a four long word burst, the state machine will continue from state R4 to the burst read sequence R5 through R10. During each pair of states (i.e., R5, R6, etc.), a new burst address is output to the EDRAM at t_{CO1s}. The output enable, chip select, and transfer acknowledge remain valid.
- *Write Sequence* — A single write cycle is performed. The size of the write (byte, word, long word) is decoded from the two lower address bits (A_{0-1}) and the SIZ_{0-1} inputs. The state machine activates the appropriate $/CAL_{0-3}$ outputs to write the correct bytes of memory. The state machine selects the row address (MAL_{0-10}, MAH_{0-10}), write mode (W/R high), and appropriate chip select ($/S_{0-3}$) signals to the EDRAM at t_{CO1s} of W1. The

transfer acknowledge is enabled during W1 to signify a zero-wait-state write. /RE is enabled at t_{CO1a}. The column address is selected at t_{CO1s} during W2. The /CAL outputs for the selected bytes and the /WE output are enabled to initiate the write cycle at t_{CO1a} of W2. The write is terminated during W3 by bringing /CAL and /WE high at t_{CO1a}. The /RE is brought high at t_{CO1a} of W4 to complete the write cycle.

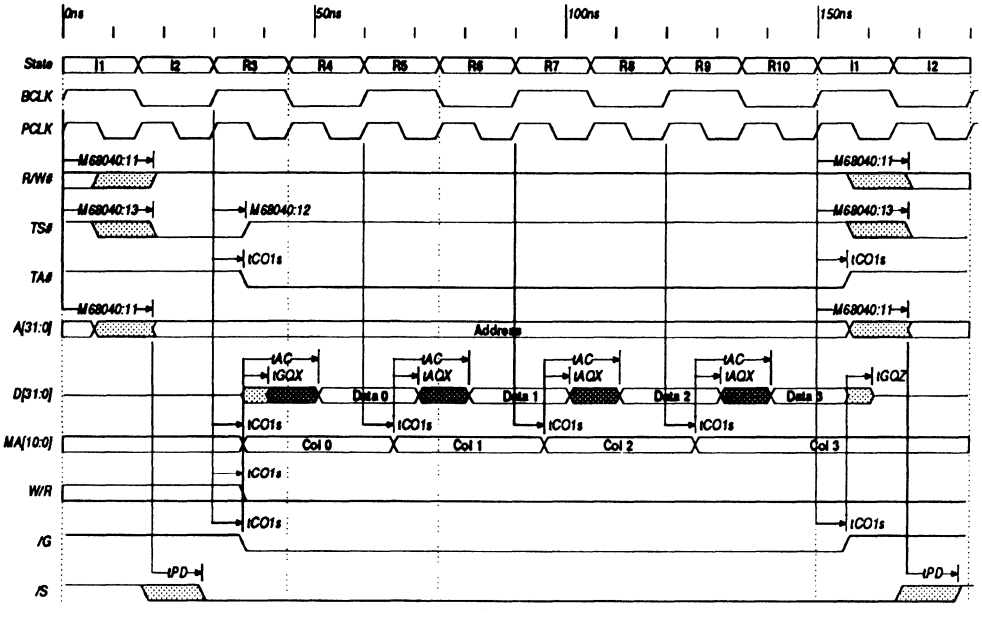
- *Burst Write Sequence* — If the transfer mode indicates a four long word burst, the state machine continues on from W4 to the burst write sequence, W5 through W10. In this case, /RE remains active to allow page mode burst writes. On each burst pair (i.e., W5, W6, etc.), a new column address is enabled to the EDRAM, and /CAL and /WE are clocked to write the next word. The /TA remains valid to acknowledge a write on each burst cycle.
- *Refresh* — If a refresh request is pending during I2, the state machine will perform an internal refresh on the next cycle by jumping to F1. Refresh mode (/F) is enabled during F1. /RE is enabled at t_{CO1a} of F1 to perform the internal refresh cycle. The cycle is terminated at t_{CO1a} of F3. The next bus event is pipelined during F3 and F4. If the next event is a read hit, the state machine jumps directly to R3 to perform the cache read while the DRAM precharge time is met. If the next event requires another DRAM cycle, the state machine jumps to I1 to allow a single wait state while the precharge time is met.

The attached burst read hit, burst read miss, and burst write timing sequences demonstrate the timing of the EDRAM controller in a 33MHz 68040 system environment with the 15ns version of the EDRAM. The same design will work at 25MHz using the lower cost 20ns version of the EDRAM. The worst case timing analysis is performed using Chronology's Timing Designer software with EDRAM timing parameter entered from the databook. EDRAM controller parameters are from the Intel 132-pin iFX780 FPGA datasheet. This FPGA was selected because of its fast clock to output delay (6ns into 30pf), fast setup time (6.5ns), and its fast address comparator feature which match EDRAM control requirements. Other FPGA or PAL devices with similar performance should also be useful to perform an EDRAM controller design. In high volume applications, this controller design should be convertible into a low cost CMOS gate array device with a recurring cost of less than five dollars. A single chip phase lock loop (PLL) clock doubler is used to provide 2X clocking for the 68040 PCLK and EDRAM controller synchronized by the 68040 BCLK.

Conclusions

A single chip EDRAM controller can be implemented using a high performance FPGA such as the Intel iFX780. This controller supports up to 16Mbytes of EDRAM without additional buffer components. Ramtron's EDRAM improves 68040 system performance by significantly reducing the number of wait states over a standard DRAM or secondary SRAM cache plus DRAM.

Burst Read Hit



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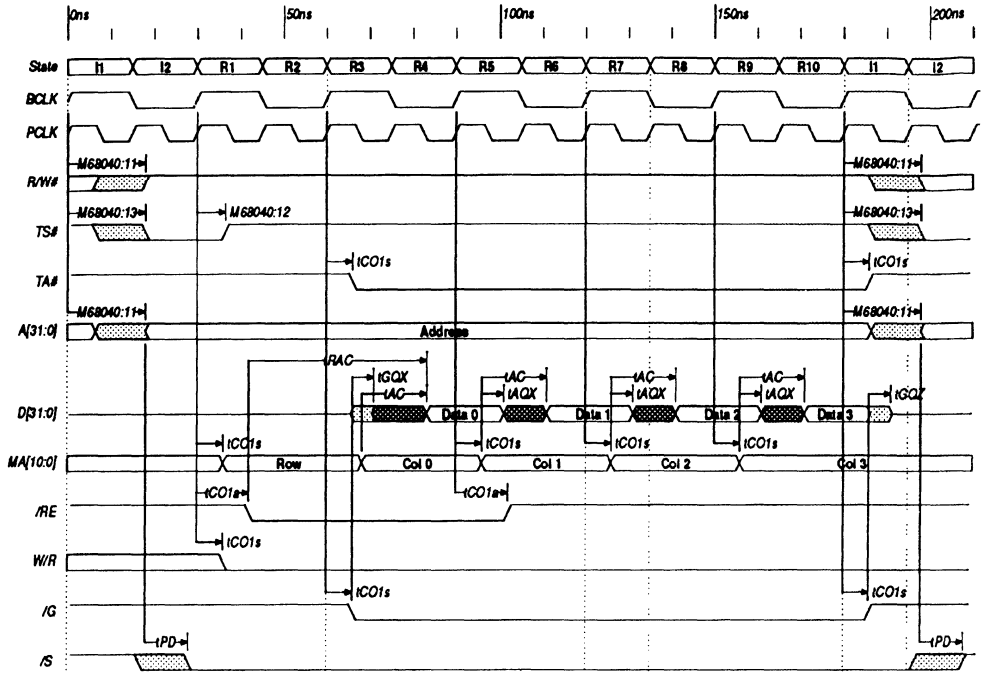
Parameter Table

Name	Min	Max	Comment
M68040:11	6.50	18	BCLK to Address, CIOUT#, LOCK#, LOCKE#, R/W#, SIZx, TLN, TMx, TTx, UPAx Valid
M68040:12	6.50		BCLK to Output Invalid
M68040:13	6.50	18	BCLK to TS# Valid
M68040:18	6.50	20	BCLK to Data Out Valid
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1d		8	CLK to Output Valid (Delayed)
tCO1a		12	CLK to Output Valid (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tAQX	5		Column Address Valid to Output Invalid
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn-off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

Burst Read Miss



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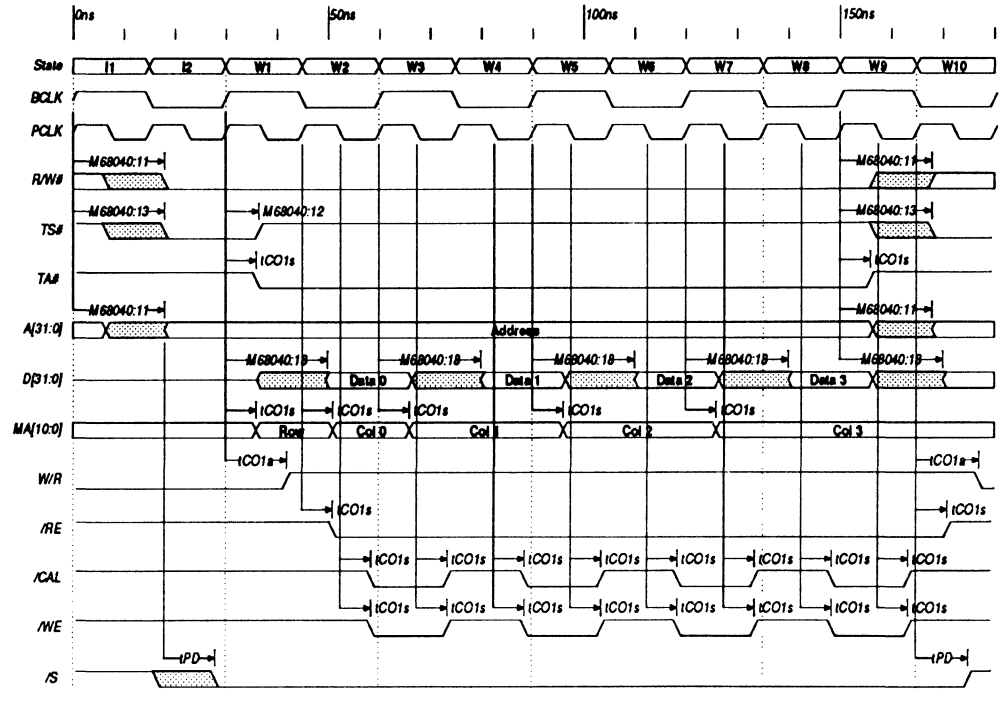
Burst Write



Parameter Table

Name	Min	Max	Comment
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tCO1d		8	CLK to Output Valid (Delayed)
tCO1a		12	CLK to Output Valid (Asynchronous)
tPD		10	Input or I/O to Output Valid
tAC		15	Column Address Access Time
tAQX	5		Column Address Valid to Output Invalid
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn-off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

EDRAM Controller For 25MHz & 33MHz IDT R3051 Microprocessors

Application Note

Summary

Ramtron's enhanced DRAM (EDRAM) is the ideal memory for high performance R3051 embedded control applications.

- No Wait States During Burst Read Hit or Write Cycles
- Only One Wait State During Burst Read Miss Cycles
- Single Chip FPGA-Based Controller Solution

Introduction

The IDT R3051 family of 32-bit RISC microprocessors is popular for high performance embedded control applications. The family includes the following members:

- R3041 — 1Kbyte Instruction, 512Byte Data Cache
- R3051 — 4Kbyte Instruction, 2Kbyte Data Cache
- R3052 — 8Kbyte Instruction, 2Kbyte Data Cache
- R3081 — 16Kbyte Instruction, 4Kbyte Data Cache, Floating Point Coprocessor

These processors use a compatible 32-bit multiplexed bus which supports single or four-word reads and single word writes. The processor clock rate options include 16, 20, 25, 33, and 40MHz.

Ramtron's EDRAM memory is the ideal main memory component to support the R3051 processors at 25 and 33MHz clock rates. Its fast 15ns read access time allows all read cycles which hit the on-chip cache to be performed in zero wait states without the need for external cache or interleaving. When a read request misses the EDRAM's on-chip SRAM cache, the EDRAM can load a new page into cache in just 35ns (a single wait state at 25 or 33MHz bus rates). Write cycles are performed in zero wait states. This high level of performance is achieved with a single non-interleaved memory bank consisting of as few as eight 1M x 4 components or a single 72-pin 4Mbyte EDRAM SIMM module. Standard DRAM memory requires the insertion of numerous wait states due to its three times slower page cycle time and two times slower random access cycle time. The EDRAM even has fewer wait states than a more complex interleaved DRAM memory subsystem as shown in figure 1.

Figure 1. Bus Cycle Comparison at 33MHz Bus Speed

Transaction	EDRAM	DRAM	Interleave DRAM
Burst Read Hit	2:1:1:1	4:2:2:2	4:1:1:1
Burst Read Miss	3:1:1:1	4:2:2:2	4:1:1:1
Write	2	3	3

A single 132-pin Intel iFX780-10 FPGA can interface 4-16Mbytes of Ramtron EDRAM main memory to a R3051 processor as shown in figure 2. This design will support either 25 or 33MHz processor clock rates by simply selecting the processor clock rate and plugging in the correct speed EDRAM SIMM modules (15ns or 20ns version). The design will also work with 16 or 20MHz versions of the R3041. This

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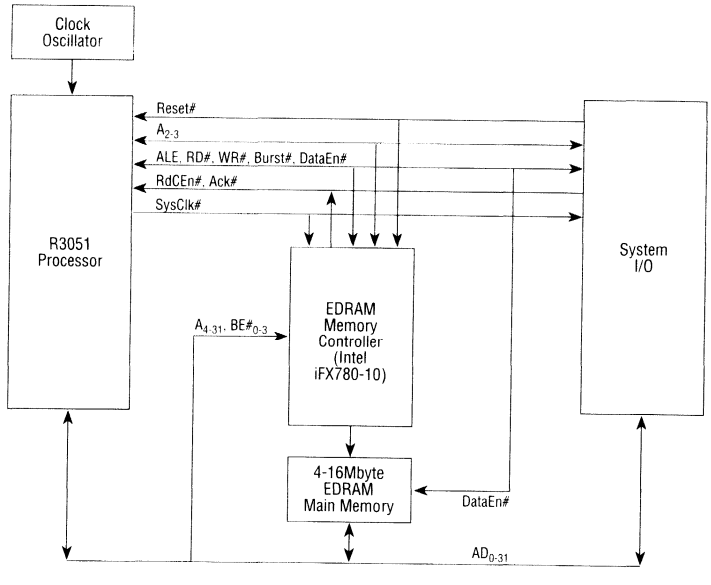
Figure 2. IDT R3051 System Block Diagram



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application note will describe the design of this 25 or 33MHz single chip EDRAM controller. A future application note will describe the design of a controller for the 40MHz versions of the R3051 family.

EDRAM Controller Design

The objective of this single chip FPGA controller design is to support all R3051 memory transactions with minimum memory wait states using a simple single phase clock design. The controller is designed to support up to four 4Mbyte EDRAM SIMM modules (DM1M32) or two 8Mbyte EDRAM SIMM modules (DM2M32) without external buffer components.

The R3051 supports the following memory transactions:

- Single 32-bit Reads
- Four 32-bit Reads
- Single Byte, Word, and Long Word Writes

In order to support these bus operations, the EDRAM controller must interface with the following processor control and address signals:

- AD_{0-31} — Address/Data Bus
- A_{2-3} — Low Address
- ALE — Address Latch Enable
- RD# — Read Enable
- WR# — Write Enable
- Burst#/WrNEAR — Burst Enable/Write Page Flag
- RdCEn# — Read Buffer Clock Enable
- Ack# — Acknowledge
- Reset#— Processor Reset
- SysClk# — System Clock Output

The controller generates the following signals to control the EDRAM SIMM modules:

- MAL_{0-9} — Multiplex Address, Bank 0-1
- MAH_{0-9} — Multiplex Address, Bank 2-3
- $MALA_{10}$ — Bank 0, A_{10}
- $MALB_{10}$ — Bank 1, A_{10}
- $MAHA_{10}$ — Bank 2, A_{10}
- $MAHB_{10}$ — Bank 3, A_{10}
- $/RE_{0-3}$ — Row Enables for Bank 0-3
- $/CAL_{0-3}$ — Column Address Latch Inputs for Bytes 0-3
- $/F_{0-1}$ — Refresh Mode Input for Low/High Banks
- W/R_{0-1} — Write/Read Mode Input for Low/High Banks
- $/S_{0-3}$ — Chip Selects for Bank 0-3
- $/WE_{0-1}$ — Write Enable for Low/High Banks

The EDRAM /G output enable signals are tied directly to the processor DataEn# output.

EDRAM Controller Functional Description

This section describes the EDRAM controller internal block diagram shown in figure 3.

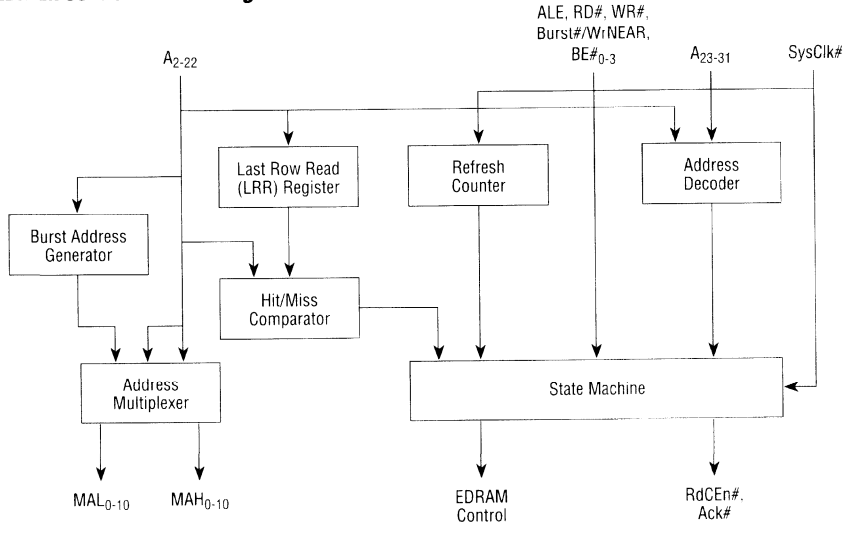
The ***Refresh Counter*** divides the SysClk# signal to generate a 62µsec refresh clock for the EDRAM. The refresh request will trigger an /F refresh on the next available bus cycle.

The ***Last Row Read (LRR) Register*** is a 13-bit register which holds the 11-bit row address and 2-bit bank address of the last EDRAM read event.

The ***Hit/Miss Comparator*** compares the new row and bank address with the LRR register on each read transaction. The state machine uses the hit/miss status to determine the EDRAM control sequence.

The ***Address Multiplexer*** selects the row address, column address, or burst address to the EDRAM multiplex address inputs under the control of the state machine. Note that two independent

Figure 3. EDRAM Controller Block Diagram



multiplex address output busses are used for MA_{0-9} to limit the capacitance driven by the FPGA. In the case of MA_{10}, individual output pins are used for each bank of memory due to the high input capacitance of this address line. The use of multiple outputs limits the clock to output delay to 8ns to achieve the goal of zero-wait-state operation at 33MHz.

The ***Burst Address Generator*** increments the lower two multiplexed address bits (MA_{0-1}) using the linear burst sequence used during R3051 cache fill cycles. The upper bits (MA_{2-8}) are identical to the column address.

The ***Address Decoder*** decodes the address bits (A_{23-31}) to determine if a valid memory address is present. The EDRAM memory is enabled for memory transactions in the lower 16Mbyte address range in this example. I/O and other memory devices are presumed to be mapped into the remaining address space.

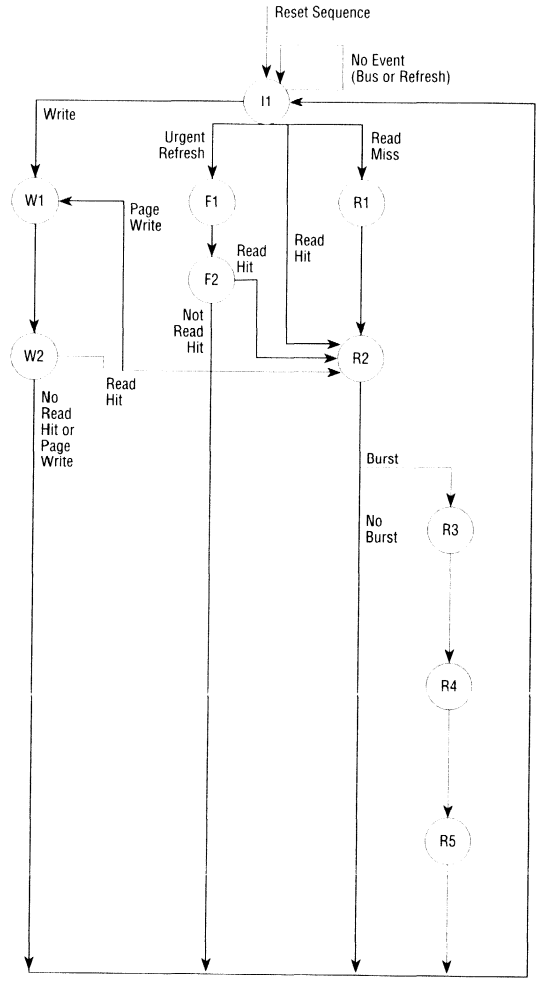
The ***State Machine*** implements the EDRAM control sequences. During reset the following sequence is run:

- *Reset Sequence* — When the Reset# input is low, the processor is in its reset state. The EDRAM controller initializes the controller logic and then enables refresh cycles. The controller will perform the required eight /F refresh cycles while Reset# is low. The required two read miss cycles per bank EDRAM initialization should be implemented in the software startup routine in the system bootstrap ROM. When Reset# is released, the controller enters its idle state waiting for memory transactions.

The detailed state diagram for the EDRAM memory sequences is shown in figure 4. A memory sequence is initiated when ALE and a valid address are present or an urgent refresh request is pending. The RD#, WR#, and hit/miss comparator status determine the final sequence for bus events:

- *Read Hit Sequence* — When a read hit is detected, the state machine will perform a single 32-bit read from the EDRAM cache. The read is executed by applying the column address (MAL_{0-8}, MAH_{0-8}) and the appropriate chip select ($/S_{0-3}$) to the EDRAM, and the RdCEn# and Ack# acknowledges to the processor during R2. All control signals are available t_{CO1s} after the falling edge of the system clock. The processor enables data onto the address/data bus using its DataEn# output.
- *Burst Read Hit Sequence* — If the Burst# is low, the state machine will continue from state R2 to the burst read sequence R3 through R5. During each state a new burst address is output to the EDRAM at t_{CO1s} after the clock. The chip select and RdCEn# outputs and processor DataEn# remain valid.

Figure 4. R3051 State Machine



- *Read Miss Sequence* — When a read miss is detected, the state machine will perform an /RE active 32-bit read from the EDRAM. During R1, the row address (MAL_{0-10}, MAH_{0-10}) and chip select ($/S_{0-3}$) are presented to the EDRAM. The /RE signal for the selected EDRAM bank is clocked t_{CO1a} after R1 to initiate a DRAM row access. This access will transfer the new row to SRAM cache. During R2, the column address is presented to read the cache location, and the RdCEn# and Ack# acknowledges are generated to the processor to acknowledge the access. The processor enables data onto the address/data bus using its DataEn# output.

- *Burst Read Miss Sequence* — If the Burst# is low, the state machine will continue from state R2 to the burst read sequence R3 through R5. During each state a new burst address is output to the EDRAM at t_{CO1s} after the clock. The chip select and RdCEn# outputs and processor DataEn# remain valid.
- *Write Sequence* — An /RE active single write cycle is performed. The bytes written are determined by the $BE\#_{0\text{-}3}$ inputs placed on the $AD_{0\text{-}31}$ bus during address output time. The state machine activates the appropriate $/CAL_{0\text{-}3}$ outputs to enable the correct bytes of memory. The state machine selects the row address ($MAL_{0\text{-}10}$, $MAH_{0\text{-}10}$) and appropriate chip select ($/S_{0\text{-}3}$) signals to the EDRAM and the Ack# acknowledge to the processor during W1. /RE is enabled t_{CO1a} after the beginning of W1. The column address is selected at t_{CO1s} of W2. The /WE and /CAL outputs for the selected bytes are enabled at t_{CO1a} of W2 to initiate the write cycle. Since the write was acknowledged during W1, it is possible for the processor to initiate another memory cycle during W2. If the next cycle is a read hit, the state machine jumps directly to R2 to perform a cache read while the EDRAM precharge occurs. If the next cycle is a read miss, the state machine inserts a single wait state by entering I1. If the next cycle is a write cycle, the state machine checks the Burst#/WrNEAR input to determine if a page write hit has occurred. On a page write hit, the EDRAM /RE output remains low and the EDRAM performs another page write cycle by jumping back to W1. The EDRAM can perform a series of zero-wait-state writes on consecutive back-to-back write cycles that are in the same page. On a write miss, the state machine jumps to I1 to insert a wait state while the EDRAM precharge occurs.
- *Refresh* — If a refresh is pending during I1, the state machine will perform an internal refresh on the next cycle by jumping to F1. Refresh mode (/F) is enabled during F1. /RE is enabled t_{CO1a} after F1 to perform the internal refresh cycle. The next bus event is pipelined during F2. If the next event is a read hit, the state machine jumps directly to R2 to perform the cache read while the DRAM precharge time is met. If the next event requires another DRAM cycle, the state machine jumps to I1 to allow a single wait state while the precharge time is met.

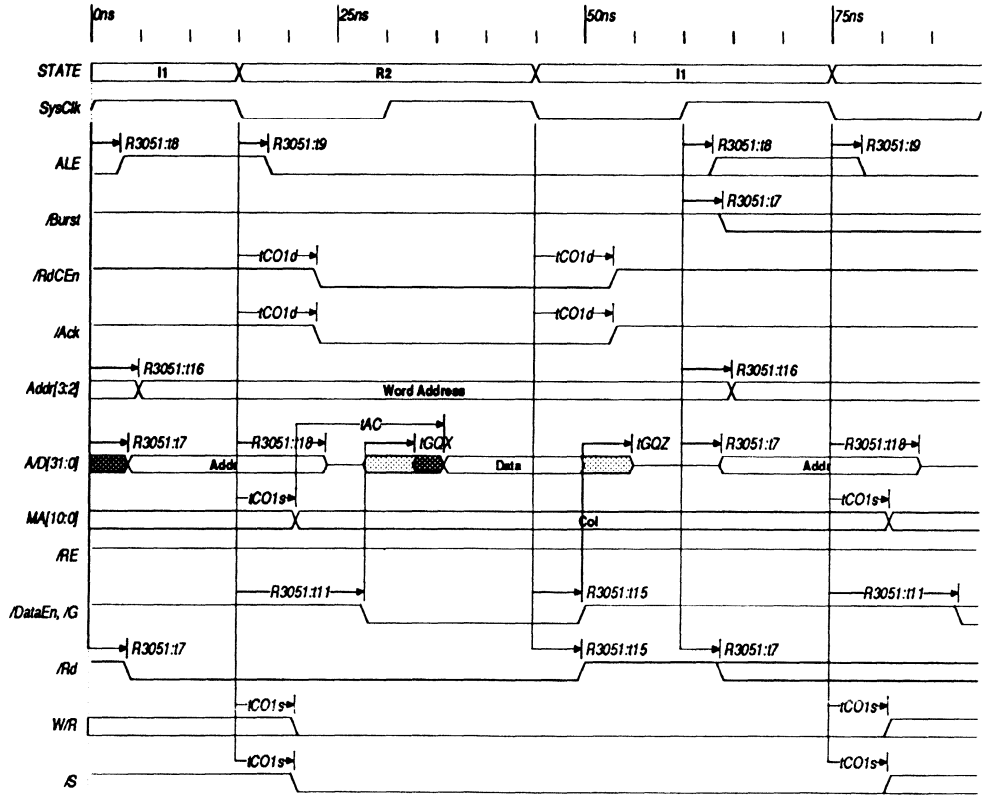
Note that the EDRAM control interface is partitioned to make sure that the output capacitance does not cause the clock to output time on any signal to exceeded 8ns. As a result, heavily loaded signals such as /F and /WE are split into two pins which drive either the low or high two banks of memory. On the other hand, the $/CAL_{0\text{-}3}$ signals are lightly loaded and a single pin drives all four banks of memory.

The attached read hit, burst read hit, read miss, burst read miss, write, and page mode write timing sequences demonstrate the timing of the EDRAM controller in a 33MHz R3051 system with the 15ns version of the EDRAM. The same design will work at 16, 20 and 25MHz using the lower cost 20ns version of the EDRAM. The worst case timing analysis is performed using Chronology's Timing Designer™ software with EDRAM timing parameters entered from the databook. EDRAM controller parameters are from the Intel 132-pin iFX780-10 FPGA datasheet. The Intel FPGA was selected because of its fast clock to output delay (6ns into 30pf), fast setup time (6.5ns), and its fast address comparator feature which allows implementation of a single chip EDRAM controller. Other FPGA or PAL devices with similar performance should also be useful to perform an EDRAM controller design. In high volume applications, this controller design should be convertible into a low cost CMOS gate array device with recurring cost of less than five dollars. A simpler version of this controller supporting up to 8Mbytes of EDRAM could be implemented using a single multiplexed address bus and fit into the lower cost 84-pin version of the Intel iFX780.

Conclusion

A single chip EDRAM controller for the 25 and 33MHz IDT R3051 microprocessor can be implemented using a high performance FPGA such as the Intel iFX780. This controller supports up to 16Mbytes of EDRAM without additional buffer components. Ramtron's EDRAM improves R3051 system performance by significantly reducing the number of wait states over a standard DRAM or interleave DRAM. This system should provide one of the fastest and most integrated embedded control solutions available.

Single-Word Read Hit



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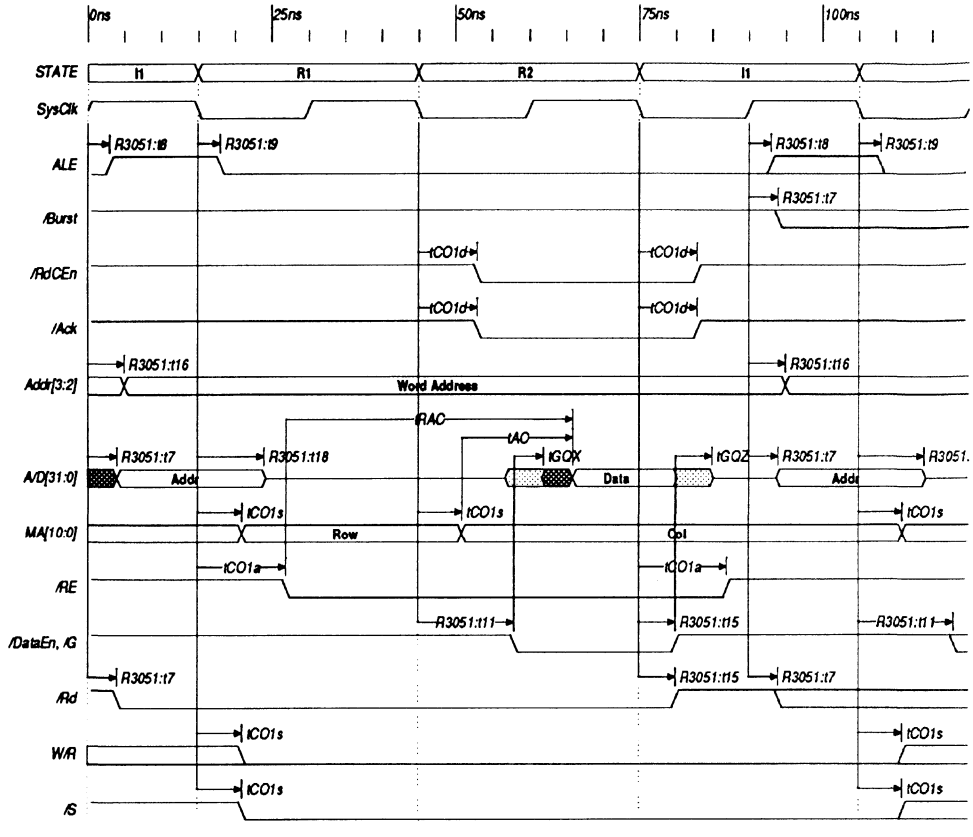
R3051:t16		5	Addr(3:2) Valid From SysClk
R3051:t18		9	A/D Tri-state From SysClk Falling
R3051:t19		10	SysClk Falling to Data Out
tCO1s		6	CLK to Output Valid (Synchronous)
tCO1d		8	CLK to Output Valid (Delayed)
tCO1a		12	CLK to Output Valid (Asynchronous)
tCLR		15	Input or I/O to Asynchronous Clear/Preset
tAC		15	Column Address Access Time
tAQX	5		Column Address Valid to Output Turn-on
tGQX	0	5	Output Enable to Output Drive Time
tGQZ	0	5	Output Turn-off Delay From Output Disabled
tRAC		35	Row Enable Access Time, On a Cache Miss

Single-Word Read Miss



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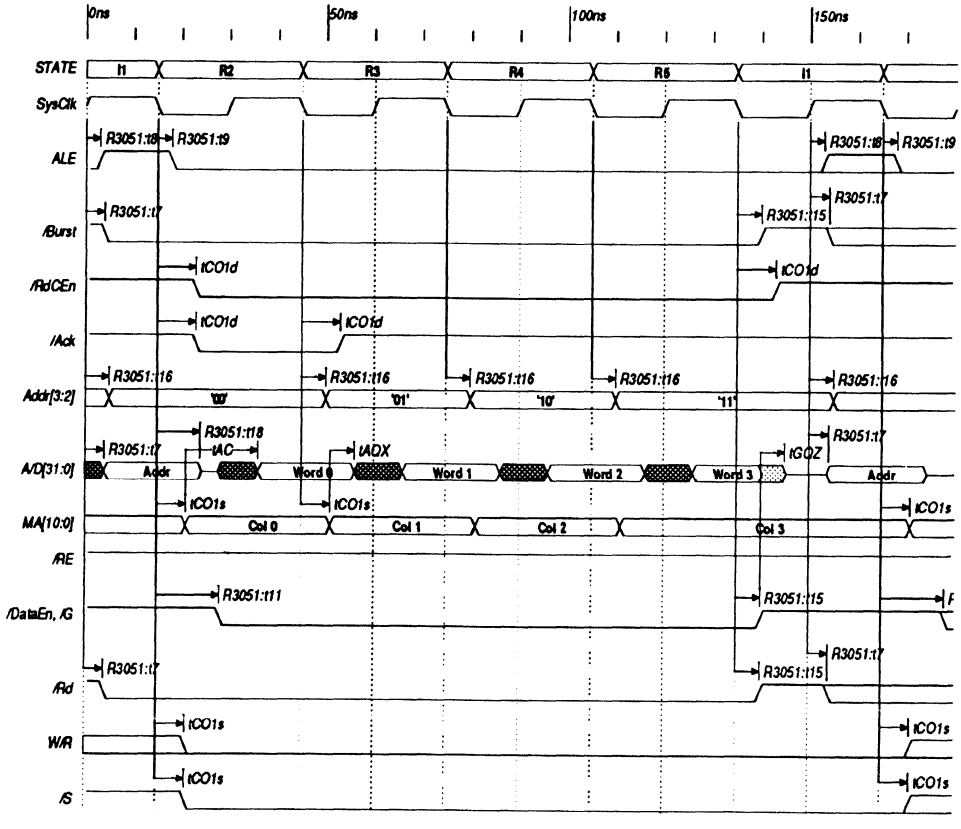
Quad-Word Read Hit



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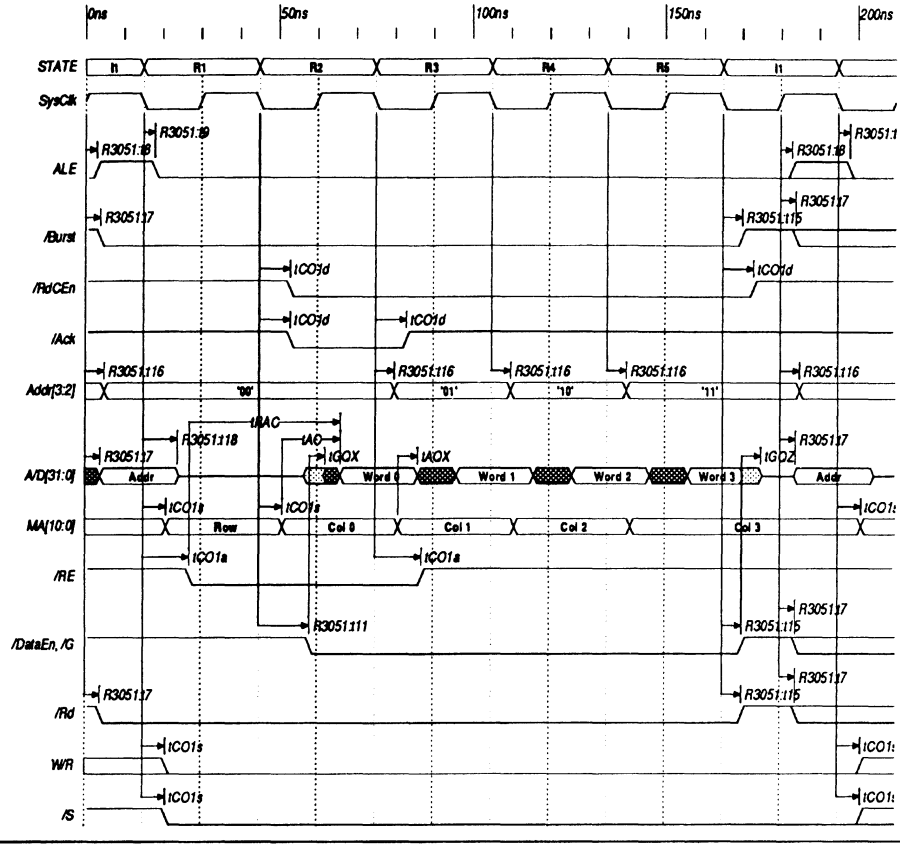
Quad-Word Read Miss



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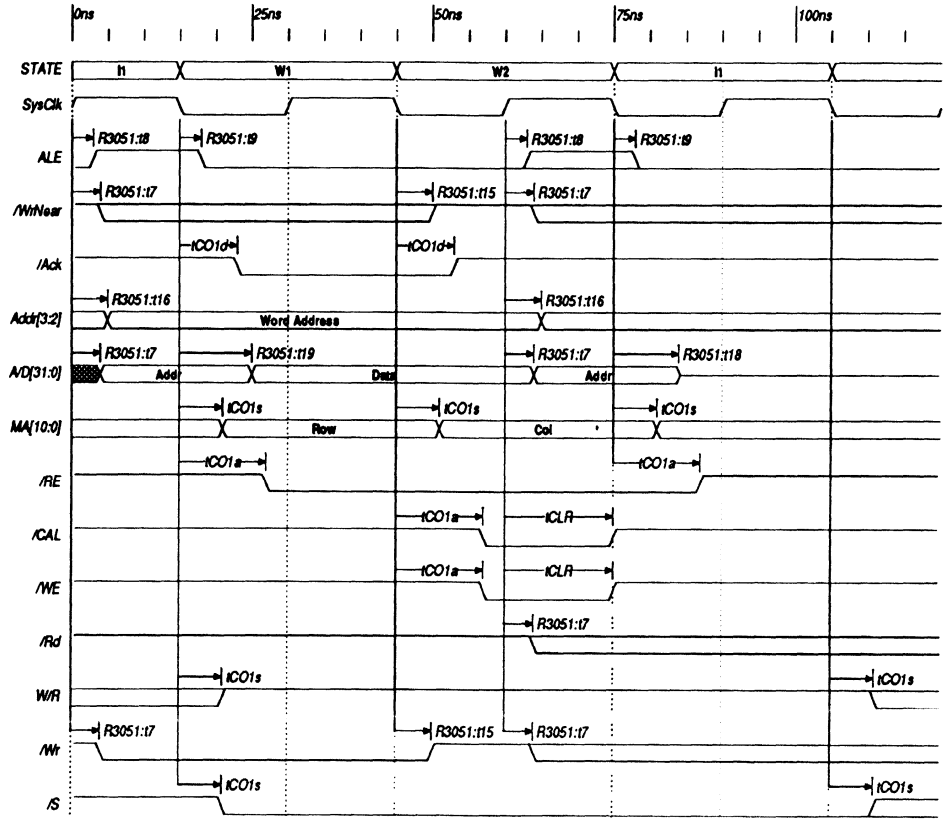
Single-Word Write



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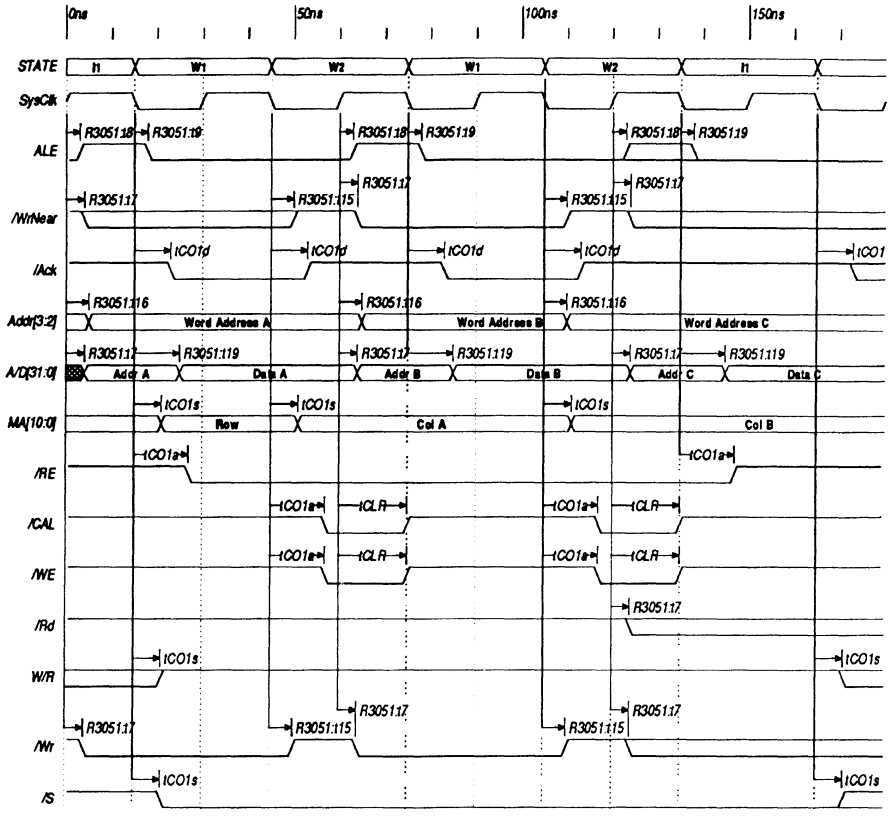
Single-Word Write Followed by Page-Mode Write



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